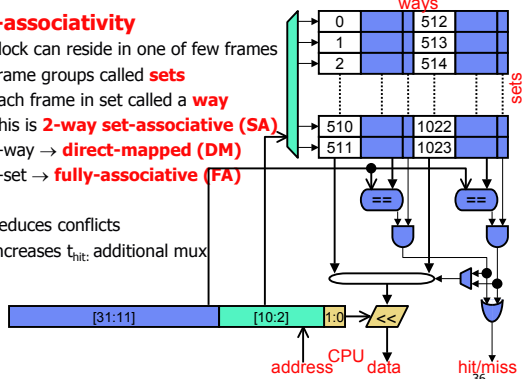


Set-Associativity

Set-associativity

- Block can reside in one of few frames
- Frame groups called **sets**
- Each frame in set called a **way**
- This is **2-way set-associative (SA)**
- 1-way → **direct-mapped (DM)**
- 1-set → **fully-associative (FA)**

- + Reduces conflicts
- Increases t_{hit} : additional mux

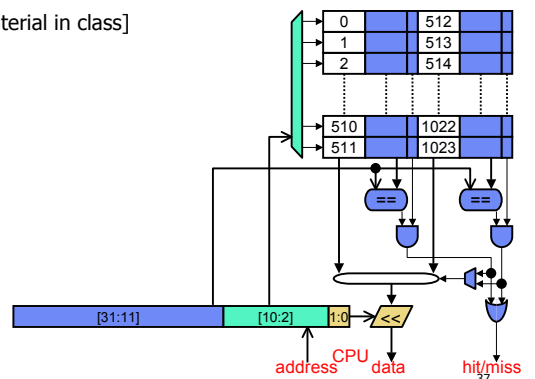


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Set-Associativity

- [material in class]



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Cache Performance Simulation

- Parameters: 32B cache, 4B blocks, **2-way set-associative**
- Initial contents : 0000, 0010, 0020, 0030, 0100, 0110, 0120, 0130

Cache contents	Address	Outcome
[0000,0100], [0010,0110], [0020,0120], [0030,0130]	3020	Miss
[0000,0100], [0010,0110], [0120,3020], [0030,0130]	3030	Miss
[0000,0100], [0010,0110], [0120,3020], [0130,3030]	2100	Miss
[0100,2100], [0010,0110], [0120,3020], [0130,3030]	0012	Hit
[0100,2100], [0010,0110], [0120,3020], [0130,3030]	0020	Miss
[0100,2100], [0010,0110], [3020,0020], [0130,3030]	0030	Miss
[0100,2100], [0010,0110], [3020,0020], [3030,0030]	0110	Hit
[0100,2100], [0010,0110], [3020,0020], [3030,0030]	0100	Hit (avoid conflict)
[2100,0100], [0010,0110], [3020,0020], [3030,0030]	2100	Hit (avoid conflict)
[0100,2100], [0010,0110], [3020,0020], [3030,0030]	3020	Hit (avoid conflict)

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Cache Replacement Policies

- [material in class]

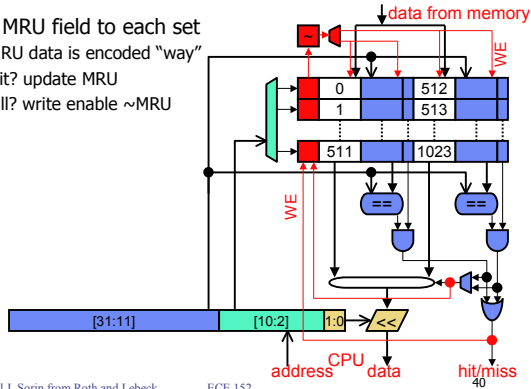
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NMRU and Miss Handling

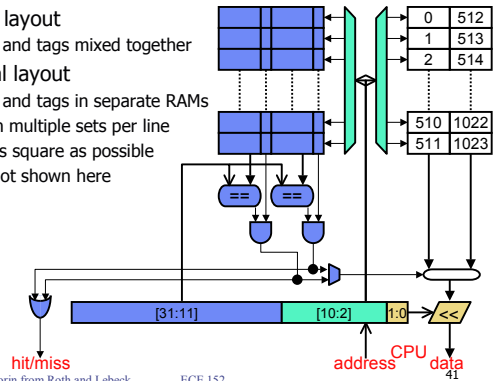
- Add MRU field to each set
 - MRU data is encoded "way"
 - Hit? update MRU
 - Fill? write enable \sim MRU



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Physical Cache Layout

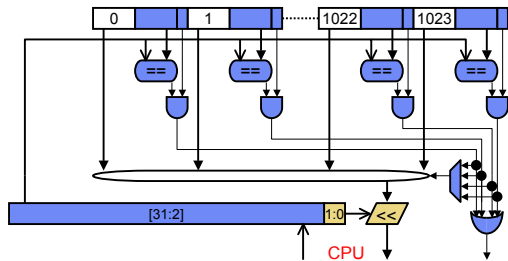
- Logical layout
 - Data and tags mixed together
- Physical layout
 - Data and tags in separate RAMs
 - Often multiple sets per line
 - As square as possible
 - Not shown here



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Full-Associativity

- How to implement full (or at least high) associativity?
 - Doing it this way is terribly inefficient
 - 1K matches are unavoidable, but 1K data reads + 1K-to-1 mux?



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