A Flexible Design Methodology for Analog Test Wrappers in Mixed-Signal SOC's

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Abstract

The manufacturing test cost for mixed-signal SOC's is widely recognized to be much higher than that for digital SOC's. It has been shown in recent prior work that the use of analog test wrappers (ATWs) for embedded analog cores in mixed-signal SOC's reduces test cost. ATWs enable analog test using digital test access mechanisms, thereby reducing the need for expensive mixed-signal testers. However, analog cores, which tend to be application-specific, evolve more than digital cores with changes in technology. The ATW specifications are therefore subject to change due to the speed/frequency requirements of the newer and faster analog cores that are embedded in the SOC. These changes in specifications require the redesign of the data converters in an ATW. We propose an automated parameter translation and ATW redesign methodology. We demonstrate the effectiveness of our methodology using a set of analog tests specified for a representative analog core. We further study the tradeoffs between test time and silicon area. Experimental results are presented for three ITC'02 benchmark SOC's that have been augmented with five representative analog cores.

1 Introduction

The test cost for mixed-signal SOC's is significantly higher than that for digital SOC's [1]. Therefore, design-for-testability (DfT) techniques that reduce mixed-signal test cost are becoming increasingly important. The use of analog test wrappers (ATWs) for embedded analog cores in mixed-signal SOC's has recently been shown to reduce test cost [2, 3]. ATWs enable analog test using digital test access mechanisms, thereby reducing the need for expensive mixed-signal testers. ATWs also allow analog and digital cores to be tested in a unified manner; this approach not only reduces SOC test time, but it also facilitates test reuse for analog cores in a "plug-and-play" manner.

The design of ATWs depends greatly on the test requirements for the analog cores. However, analog cores are application-specific and tend to evolve more than digital cores with a change in technology [4]. This change in analog cores is accompanied by a change in their test specifications. Changes in test specifications require the redesign of the wrapper, in particular the pair of A/D and D/A data converters in the ATW. An efficient redesign methodology is therefore needed to facilitate rapid resynthesis of the ATWs when the performance specifications of an analog core change. This is essential to ensure that ATW redesign does not stall the quick integration of analog cores in mixed-signal SOC's in a "plug-and-play" manner. While the authors in [2] and [3] demonstrated the efficient use of ATWs in mixed-signal SOC's, they did not address the important issue of ATW redesign.

The DAC and ADC used in ATWs are mixed-signal circuits that need to be optimized for speed, resolution, frequency requirements,

and area overhead. This optimization requires careful design selection and parameter optimization for the DACs and ADCs. The first step in wrapper design involves parameter translation from the analog test specifications to the parameter specifications for the wrapper's ADC and DAC. The test specifications include maximum test frequency, sampling frequency, number of samples, test accuracy, and the test analysis method; the data converter specifications include signal-to-noise ratio (SNR), total harmonics distortion (THD), differential non-linearity (DNL), integral non-linearity (INL), and spurious-free dynamic range (SFDR). These data converter parameters affect test accuracy, test time and the silicon area of the wrapper.

In this paper, we propose a design methodology for the wrapper data converters that avoids extensive redesign of analog wrappers with changing specifications. Our goal is to reduce the design effort by taking advantage of partial synthesis of data converters. An effective automated parameter translation method is critical to the proposed redesign methodology. The proposed parameter translation method maps test specifications to the parameter specifications for the data converters. We present the parameter translation method in detail, and demonstrate its effectiveness using simulation results. These results are presented for a set of analog tests specified for five representative analog cores. We further use parameter translation in conjunction with a test scheduling method in an iterative manner to reduce the area of the ATWs without impacting the overall SOC testing time.

The rest of this paper is organized as follows. In Section 2, we give an overview of related work. Section 3 presents the design methodology for the data converters in analog test wrappers. In Section 4, the parameter translation method is presented. We detail the tradeoffs between the data converter area and test time in Section 5. In Section 6, we present results of parameter translation for a representative analog core detailed in [3]. Finally, we conclude the paper in Section 7.

2 Related work

In the analog testing domain, significant research has been done to eliminate the need for an expensive analog or mixed-signal ATE. The use of on-chip data converters, proposed in [6, 7], obviates the need for expensive analog testers. Several BIST techniques have also been proposed for mixed-signal blocks that cannot be directly tested by an ADC-DAC pair. Such BIST techniques target either data converters themselves [8, 9, 10, 11] or phase-locked loops [12]. Recently, in [2], test wrapper design for analog cores has been developed to obviate the need for mixed-signal testers. The analog test wrappers contain on-chip data converters that convert analog cores into virtual digital cores.

Figure 1 shows a block diagram of the analog test wrapper proposed in [2]. The control and clock signals generated by the test control circuit are highlighted. The registers at each end of the data converters are written and read in a semi-serial fashion depending on the frequency requirement of each test. The digital test control circuit selects the configuration for each test. This configuration includes the divide ratio of the digital test access mechanism (TAM) clock, the serial to parallel

¹This research was supported in part by the Semiconductor Research Corporation under contract no. 2004-TJ-1174.

Figure 1. Block diagram of the analog test wrapper [2].

conversion rate of the input and output registers of the data converters, and the test modes. The test modes of the wrapper include a normal mode, a self-test mode and a core-test mode. In [3], the authors used the ATW in a cost-optimization approach to reduce the overall SOC test cost.

A considerable amount of research has also been carried out on data converter design and synthesis [13, 14]. Several analog synthesis tools have also been developed [15, 16]. The availability of well-developed and automated design and synthesis tools has made the integration of on-chip data converters feasible. However, there is a need for a design methodology for the ATW data converters that allows the reuse of existing components and the quick integration of wrapped analog cores in mixed-signal SOCs.

3 ATW redesign methodology

The ATW consists of two types of modules, namely the digital modules and the mixed-signal data converters. The registers, encoder, decoder and the control block are the digital modules; even though they change slightly with a change in analog core specifications, they can be easily synthesized. Commercial synthesis tools can be readily used for the design of the digital modules. These modules are designed to meet the bandwidth and frequency requirements of the analog test. This design phase requires a relatively small design effort compared to the analog part of the ATW. The analog part comprises mainly of the ADC and DAC. The design of these data converters is the most challenging part in the design of the ATW.

The design of analog circuits is typically knowledge-based, thus it is hard to automate. In data converter design, we can choose from several architectures; each architecture has a large number of configurations due to the choice of different transistor sizes. In addition, each architecture caters to a different spectrum of performance specifications. For example, flash converters are suited for high-speed applications that require low resolution (less than 8 bits) and Sigma-Delta ($\Sigma - \Delta$) converters are suited for high resolution, but lower-speed relative to the flash converters. Hence, the complete redesign of wrappers for analog cores can be prohibitively expensive and time-consuming.

The proposed redesign methodology exploits the availability of libraries of pre-designed components in most design houses. Most companies develop and maintain a library of generic analog building blocks such as OPAMPs, comparators, differential amplifiers, as well as circuits such as ADCs and DACs. Typically, several architectures of the same components co-exist in the library, e.g., the library can consist of flash, pipelined, successive-approximation, and Sigma-Delta ADCs [17]. The library also consists of building blocks for each architecture, e.g., switches, multiplexers, OPAMPs, and current sources. These building blocks are optimized for a particular operating point, bias condition and frequency. During architectural synthesis of the ATWs, we use the information in the library to select the data converter and its components, and estimate the performance of the ATW. During

Figure 2. Illustration of the redesign methodology.

circuit synthesis, we consult the library to optimize the performance of data converter blocks for the necessary operating conditions.

Figure 2 illustrates the flow of the proposed redesign methodology. We start with the test specifications for the analog core, which are given in terms of test signal attributes (namely frequency, power, and shape), the desired test accuracy, the response analysis method (histogram measurement, spectral analysis, and amplitude measurement), and the desired number of samples. These test specifications are used to determine the parameters for the data converters. An automated parameter translation method maps the test specification to data converter parameters such as resolution, frequency, DNL, INL, SINAD, SNR and SFDR. Based on these specifications, an appropriate architecture for the data converters is selected from the library such that its on-chip implementation can meet the desired resolution and frequency requirements. At this point, it is also possible to select multiple architectures that can potentially meet the specifications. Since the relationship between performance and area is not monotonic, we explore more than one architecture to achieve area-efficient designs. For example, a simple comparator circuit may need to be extensively resized, i.e., the transistors have to be made very wide, to reduce the propagation delay to an acceptable level; on the other hand, a slightly more complicated architecture can be realized using smaller transistors. Thus, it may be advantageous to employ a more complicated architecture with smaller device sizes.

The architectural synthesis module uses a commercial tool to synthesize the selected architectures; it uses building blocks from the component library. Next, a circuit simulator is used to fine-tune and optimize the design for the desired parameters of the data converters. The three main goals of the circuit optimization step are:

1. Optimize data converter building blocks with respect to the given

bias and input conditions.

2. Optimize the performance of data converter building blocks, particularly for smaller-area architectures.
3. Minimize the area of the overall architecture by reducing the sizes of building blocks whose performance exceeds the requirements.

As an example, consider two candidate architectures that deliver 8-bit resolution: an 8-bit flash ADC, and a 2-stage pipelined ADC with 4-bit flash ADC stages. While the functionality of the data converters for these two architectures are identical, the operating conditions are different since the comparators within the flash ADC need to respond to much smaller input steps and have smaller gray zones. Thus, they rely on dramatically different architectures. Therefore, the optimization required for the two architectures differs and both can be used to satisfy different specifications. The 8-bit flash ADC has a larger area than the 2-stage pipeline ADC, however it can be optimized to be faster than the 2-stage pipeline ADC [17]. Depending on the requirements, one of the two architectures can be optimized.

Circuit optimization is carried out in an iterative manner. After each optimization step, the overall circuit is synthesized and simulated to extract the performance specifications. If the parameters of the data converters match the required parameters given by the translation method, the redesign procedure is deemed to be complete.

In the proposed redesign procedure, the synthesis modules shown in Figure 2 are relatively easy to implement, since a wide range of commercially-available synthesis tools can be used. The automation of the parameter translation module however has not been addressed in prior work. Therein lies the main contribution of the paper.

4 Parameter translation

In this section, we describe the parameter translation method that maps the test specifications to the data converter parameters. The translation method is central to the overall effectiveness of the redesign methodology; it plays a key role in determining an ATW design that results in the desired test accuracy and test time for the analog core. An effective translation method ensures that the redesign flow results in data converters that meet the desired test accuracy.

Recall that the data converter parameters that we determine, namely SNR, SFDR, DNL, and INL, are based on the test signal attributes such as frequency, power, shape, number of samples, and the desired test accuracy. It is difficult to obtain a precise direct analytical relationship between these test specifications and the data converter parameters due to non-linearities and random noise that are introduced in practice. Hence, we use MATLAB macros to model behavioral and performance characteristics of the data converters. These data converter models are used to determine the data converter parameters for the given set of test specifications.

Figure 3 illustrates the flow of the proposed translation methodology. We start with an initial behavioral model that has a pre-defined resolution, frequency, DNL, and inherent noise level. These specifications of the initial model are obtained through coarse analytical calculations using the given test specifications. For a specified sampling frequency, there is typically a range of data converter resolutions available in the data converter library. We consult the library and use the required test accuracy to determine the resolution (within the available range) and DNL error for the data converter model. Using the initial

Figure 3. Illustration of the parameter translation methodology.

Figure 4. Block diagram of the MATLAB behavioral model for an ADC.

estimation of the resolution and DNL error, the “Converter Selector” generates a model of the ADC.

The test specifications are also used to generate the input to the data converter model. The output of the data converter is then analyzed to determine the test accuracy and the remaining specifications of the data converter. If the test accuracy is within a user-defined quantity ϵ of the specified accuracy, the test specifications are deemed to have been satisfied, and the translation process is complete. However, if the desired accuracy is not achieved, some of the data converter specifications are modified. First, the DNL error is decreased based on the DNL error of a corresponding ADC in the data converter library. Next, the noise level is decreased. If the desired accuracy is still not achieved, the resolution is increased. This is done in an iterative manner until the desired accuracy level is reached.

If the achieved accuracy is greater than the specified accuracy by δ , which is a user defined quantity, the resolution is reduced by one bit for the next iteration. This is done to ensure that the lowest-area data converter is selected to satisfy the test accuracy requirement. If the accuracy is not achieved in the next iteration with a reduction of one bit, the algorithm terminates by rolling back to the previous result. This feature is not shown in Figure 3 for the sake of simplicity.

The MATLAB behavioral model consists of two parts. First, random noise is injected based on the initial SNR calculation. Next, non-linearities are inserted as DNL error to the conversion lookup table. Figure 4 illustrates the block diagram for the MATLAB behavioral

Figure 5. Accuracy measurement for the cut-off frequency test.

model for an ADC.

The test accuracy is measured by comparing the applied input signal with the output response of the data converter. For an ADC, the applied input signal has the shape, frequency and power of the expected response of the analog core, and the analysis method is part of the test specifications. Similarly, for a DAC, the input signal to the DAC is the digitized test signal for the analog cores. We use examples of ADCs to explain our proposed methodology. The proposed method is not limited to ADCs; it is applicable to DACs in the same manner.

As an example of the measurement of test accuracy, we illustrate accuracy measurement for a cut-off frequency test in Figure 5. Spectral analysis is used for this test. The accuracy is measured as the percentage difference in the cut-off frequency measurement from the input signal V_{in} and the cut-off frequency measurement from the output signal V_{out} . The input signal is a three-tone signal generated from the given test specifications, and the cut-off frequency is measured by the method of extrapolation. Using this measurement technique, the input to the data converter and the output signal from the data converter result in cut-off frequencies of 61KHz and 58KHz, respectively. There is a 5% difference in the two measurements, thus the test accuracy is 95%.

The test accuracy specification, together with the other specifications are used in the initial coarse analysis. For example, if a gain test requires 98% test accuracy, and the amplitude of the input signal is 0.8V, the resolution and DNL are calculated as follows.

A 98% test accuracy implies that a maximum of 2% error is permissible, i.e., a maximum error of $0.8 \times 0.02 = 16\text{mV}$ is allowed in the amplitude measurement. Thus for an ADC, the following relationship has to be satisfied: $1\text{LSB} + \text{DNL} < 16\text{mV}$, where 1 least significant bit (LSB) equals $V_{\max}/(2^R - 1)$; $V_{\max}$ is the full range of the ADC, and R is the resolution. The DNL error range should be between 0.2LSB and 0.5LSB. Thus, for $V_{\max} = 2.6\text{V}$, the lowest value of R is determined to be 8 bits. Having determined R , the SNR for a full-scale sine wave is calculated as [18]:

$$\text{SNR}_{dB} = 6.02 \cdot R + 1.763 \quad (1)$$

The SFDR can also be approximated as $9 \cdot R$ [18]. Thus, the macro model provides the initial parameters that can be further tuned based on the requirements.

5 Tradeoffs between test area and test time

In this section, we study the trade-off between wrapper area and SOC testing time. We show that the area of the ATW can be reduced at the expense of an increase in the testing time of the analog core under consideration. However, test scheduling methods at the full-chip level

Figure 6. Illustration of the measurement of signal-to-noise floor SN_f .

can be used to ensure that the increase in the core testing time does not have a significant impact on the overall SOC testing time.

A large number of tests for analog cores use spectral analysis methods, which rely on the measurement of the fundamental frequencies in the output response. The noise floor Nf in the frequency bin of the fundamental frequency affects the overall test accuracy. The noise floor is the average of magnitude of the signal in the frequency bins excluding the fundamental frequency. For example, Figure 6 illustrates the noise floor for the frequency spectrum.

For an ADC driven by a sinusoidal input, the theoretical noise floor Nf_{th} is given by:

$$Nf_{th} = \text{SNR}_{dB} + 20 \log_{10}(N_s/2),$$

where N_s is the total number of samples and SNR_{dB} is as defined in Equation (1) [18].

SNR_{dB} decreases by 6.02dB with a 1-bit decrease in the ADC resolution. In (3), this decrease can be offset by increasing the number of samples N_s . Let k represent the factor by which N_s should be increased to maintain the same accuracy, even with a 1-bit decrease in resolution R . Thus, we need to determine the value of k that satisfies the following relationship:

$$\begin{aligned} 6.02 \cdot R + 1.76 + 20 \log(N_s) \\ = 6.02 \cdot (R - 1) + 1.76 + 20 \log(N_s \cdot k). \end{aligned} \quad (2)$$

From (3), we have $k = 1.99$. This implies that for every 1-bit decrease in the resolution of a data converter the total number of samples needs to be increased by a factor of 2 to maintain the same noise floor, which in turn can impact test accuracy. Note that for all ADC architectures, a 1-bit decrease in R reduces the area of the ADC at least by a factor of $1/R$ [17].

The increase in the number of samples impacts the test time of the core. The test time of a core is directly related to the number of samples of the applied test signals as follows [2]:

$$T = N_s \cdot f_{TAM} / f_s, \quad (3)$$

where f_{TAM} is the digital TAM frequency and f_s is the sampling frequency. In core-based testing, the time for the SOC is determined by the full-chip test schedule that includes all the cores. Typically, every test schedule has some idle time. The idle time can accommodate some increase in the testing time of the individual cores without significantly

Test	V_{amp}^1	f_{max}^2	f_s	N_s	Acc^3
G_{pb}	1.8V	50kHz	1.5MHz	1500	98%
f_c	1.8V	800kHz	15MHz	2024	95%
G_{1MHz}	80mV	2MHz	8MHz	4096	90%
IIP_3	16mV	250kHz	8MHz	4096	95%

¹ V_{amp} : minimum signal amplitude(s); ² f_{max} : maximum signal frequency; ³ Acc : test accuracy.

Table 1. Test requirements for Cores A and B (I-Q transmit).

Figure 7. Illustration of IIP_3 measurement.

impacting the total SOC test time. Thus, an increase of t clock cycles in the core test time does not necessarily imply an increase of t clock cycles in the SOC testing time. This observation allows us to optimize the area of the ATW by reducing the resolution of the data converters, without significantly increasing the SOC testing time.

In Section 6, we use the parameter translation method in conjunction with an existing TAM optimization and test scheduling approach to demonstrate the impact of reduction in data converter resolution on SOC testing time. For every 1-bit decrease in the data converter resolution, the parameter translation method is used to determine the remaining parameters in accordance with the test specifications. Next, the TAM optimization method from [19] is used to determine the overall SOC testing time.

6 Experimental results

In this section, we present experimental results for one of the representative analog cores, as presented in [3]. We consider the tests shown in Table 1 for Cores A and B. The tests include gain test G_{pb} , gain test at 1MHz (G_{1MHz}), cut-off frequency test f_c , and the third-order intercept test IIP_3 . The test specifications for each of the tests are listed in Table 1. The test accuracy measure for the gain tests is obtained by measuring the percentage difference in the amplitude of the data converter input signal and the amplitude of the output signal of the data converter. The cut-off frequency measurement is carried out as shown for the example in Section 4. The IIP_3 test response is measured as shown in Figure 7.

First, we use the parameter translation method to obtain the ADC parameters as presented in Table 2. The number of iterations taken to arrive at the final results is less than 4 for every test. The G_{pb} and f_c tests require a data converter resolution of 5 bits, while the G_{1MHz} and IIP_3 tests require a resolution of 10 bits. Since the analog core requires a data converter that satisfies the requirements for all the tests, the chosen data converter specs are that for the maximum resolution and sampling frequency. Thus, for Cores A and B, the data converter specifications for the IIP_3 test is chosen, i.e., the final chosen resolu-

Test	R (bits)	DNL_{max} (LSB)	Acc (%)	SFDR (dB)	T (clock cycles)
G_{pb}	5	0.30	97.95	33	50000
G_{1MHz}	10	0.25	90.20	42	12650
f_c	5	0.27	95.01	41	13653
IIP_3	10	0.25	94.50	59	25600

Table 2. Parameter translation for tests for Cores A and B.

Gain test G_{pb}

1. Coarse Analysis results: $R = 7$ bits; $DNL < 0.5$ LSB; $SNR = 44$ dB.
2. **Iteration 1:** Start with 7-bit ADC macro.
3. $DNL = 0.33$, $Acc = 98.54\%$;
5. **Reduce R**
6. **Iteration 2:** Start with 6-bit ADC macro
7. $DNL = 0.30$ LSB; $Acc = 98.10\%$
8. **Reduce R**
9. **Iteration 3:** Start with 5-bit ADC macro
10. $DNL = 3.51$ LSB; $Acc = 97.10\%$
11. **Reduce DNL**
12. $DNL = 0.3082$; $Acc = 97.95\%$;

Figure 8. Parameter translation for gain test G_{pb} for Core A.

tion is 10 bits.

To illustrate the flow of the parameter translation method, we present the details of the simulation for the gain test G_{pb} in Figure 8. The values for the user-defined parameters are $\epsilon = 0.5$ and $\delta = 0.05$. Since the first two iterations result in a higher accuracy than specified, the resolution is further decreased; the desired accuracy with the bounds of ϵ and δ are reached in the third iteration.

Next, we study the change in core test time with a change in the number of samples, while maintaining the same test accuracy. Recall that from (3), we have established that the the resolution can be decreased at the expense of an increase in the number of test samples. We use this relationship to decrease the resolution requirement of 10 bits for tests G_{1MHz} and IIP_3 for Cores A and B. Since the search space for the resolution of the data converters is very small, we can do a binary search for the appropriate resolution. In our case, we consider data converters with resolution between 4 and 12 bits. From (3), an n -bit decrease in data converter resolution increases the number of samples by $2 \cdot n$. From our simulations, we found that the 10-bit requirement for G_{1MHz} and IIP_3 could be reduced to 8 bits. Similarly, since a data converter of 8-bit resolution is going to be used for all the tests, we decreased the number of samples required for G_{pb} and f_c by increasing the resolution to 8 bits. Table 4 illustrates the change in number of samples N_s with the change in the resolution for all the tests. Although the net increase in the total number of clock cycles is 120471, the data converter area is reduced significantly. For example, if the resolution of a flash ADC is reduced from 10 bits to 8 bits, the reduction in area is 75%. This is because the area is halved for every 1-bit decrease in resolution. Similarly, for a pipeline ADC architecture that uses two smaller flash ADCs, a 2-bit reduction in resolution results in a decrease of 50% in area. Table 3 shows the decrease in the number of comparators for the two ADC architectures with a 2-bit decrease in resolution. The area of the ADCs in $0.5\mu m$ technology is also presented. The comparators are the main contributor to the overall area of the ADC; each comparator is a 10-transistor two-stage differential amplifier.

We study the impact of the increase in core test time on the overall SOC testing time. The flexible-width TAM architecture presented in [19] is used for these experiments. We use the experimental set-

R (bits)	Flash ADC		Pipeline ADC	
	# comparators	Area	# comparators	Area
10	1024	34 mm ²	64	2.81 mm ²
8	256	8 mm ²	32	1.04 mm ²

Table 3. Results for the decrease in ADC area with decrease in ADC resolution.

Test	Original parameters			New parameters			$T_{\text{new}} - T$ (clock cycles)
	R	N_s	T	R	N_s	T_{new}	
	(bits)	(samples)	(clock cycles)	(bits)	(samples)	(clock cycles)	
G_{pb}	5	1500	50,000	8	512	17067	-32933
G_{1MHz}	10	2024	12,650	8	8096	101200	88550
f_c	5	4096	13,653	8	512	1707	-11946
IIP_3	10	4096	25,600	8	16384	102400	76800

Table 4. ADC resolution versus test time for Cores A and B.

SOC p22810m			
W	T_1 (clock cycles)	T_2 (clock cycles)	ΔT (%)
24	378532	397303	4.90
32	299785	300492	0.23
40	299785	299785	0
48	299785	299785	0
56	299785	299785	0
64	299785	299785	0
SOC p34392m			
24	838643	838643	0
32	579673	609454	5.1
40	544579	544579	0
48	544579	544579	0
56	544579	544579	0
64	544579	544579	0
SOC p93791m			
24	1345978	1353913	0.58
32	1023448	1032480	0.88
40	797953	848807	6.3
48	652899	676934	3.6
56	584955	597293	2.1
64	543598	553058	1.7

$$\Delta T = \frac{T_1 - T_2}{T_2} \times 100;$$

Table 5. Testing time (in clock cycles) and percentage change in testing time using the proposed approach.

up from [3]. Digital SOC's from the ITC'02 SOC test benchmarks, namely p22810, p34392, and p93791 are augmented with five analog cores to form mixed-signal SOC's p22810m, p34392m, and p93791m. The analog cores consist of a pair of baseband I-Q transmit path with a bandwidth of 500kHz, a CODEC audio path with a bandwidth of 50kHz, a baseband down conversion path, and a general purpose amplifier. These analog cores are taken from a commercial baseband cellular phone chip. The test set specifications for each of these analog cores are given in [3].

The new testing times T_{new} from Table 4 for Cores A and B are considered for the SOC's p22810m, p34392m, and p93791m. In Table 5, the results for the SOC testing time for several TAM widths W are presented for the three SOC's. The testing time T_1 includes the test time T from Table 4 for Cores A and B, while T_2 includes the test time T_{new} for Cores A and B. The testing time T_2 for the SOC's with the lower data converter area is compared with the original test-

ing time T_1 . It is observed that in p22810m and p34392m, for several TAM widths, there is no change in the overall test time. This is due to the presence of bottleneck cores that dominate the testing time for the SOC's. However, even for p93791 that does not contain a bottleneck core, the increase in test time is very small. Based on these results, we conclude that it is possible to reduce the ATW area for the analog core without comprising the test accuracy and significantly impacting the SOC testing time.

7 Conclusions

We have presented a redesign methodology based on the partial resynthesis of data converters. We have also presented a parameter translation method that maps test specifications to the parameter specifications for the data converters in the test wrappers. Simulation results for representative analog cores demonstrate the effectiveness of the method. We have also shown that for a specified test accuracy, the ATW area can be reduced with a small increase in test time. We used parameter translation in conjunction with a test scheduling method in an iterative manner to reduce the area of the analog test wrappers, without increasing the overall SOC testing time.

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