

# A Deterministic Scan-BIST Architecture with Application to Field Testing of High-Availability Systems\*

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## Abstract

*We propose an autonomous, deterministic scan-BIST architecture that allows compact, precomputed test sets with complete fault coverage to be used for field testing. The use of such short test sequences is desirable in safety-critical systems since it reduces the error latency. It also reduces testing time and therefore allows periodic field testing to be carried out with low system downtime. We synthesize the BIST logic for several ISCAS 89 benchmarks and industrial circuit modules and show that the BIST overhead is low in all cases. The proposed design can also be efficiently used with a mixed-mode BIST strategy.*

## 1 Introduction

On-line and periodic field testing are essential to ensure the reliable operation of computer-controlled systems. Protection against field failures is especially important for the control of critical automotive functions, railway control, satellites, avionics, telecommunications and medical electronics. The stringent safety and availability requirements of such applications pose a significant challenge for designers and test engineers.

Built-in self test (BIST) is being increasingly used for production testing of VLSI circuits [1]. In BIST, extra logic is included on-chip to generate test patterns and compact test responses. BIST structures for off-line production testing have usually been different from those used for on-line testing. A typical off-line BIST scheme uses a STUMPS architecture, in which a linear feedback shift register (LFSR) feeds the scan chains and the test responses are compressed using a multiple input signature register (MISR); see Figure 1 [2]. If the scan chains are directly fed by the LFSR, they can contain highly correlated patterns, which in turn can adversely affect the fault coverage. Therefore, a phase shifter consisting of exclusive-or gates is often employed; the phase shifter reduces the correlation between the test patterns feeding the different scan chains [3]. In contrast to off-line BIST, on-line BIST structures typically include replicated hardware, comparators and checkers since they are based on space, time or information redundancy [4].

For an off-line BIST scheme to be useful for periodic testing, it should guarantee very high fault coverage. In addition,

it should require small testing time so that the test can be completed within the short idle intervals during field operation. This is especially important for systems that must provide high availability. This necessitates a BIST architecture that applies a compact, precomputed test sequence to the circuit under test (CUT). Pseudorandom methods [5] and test set embedding approaches [6,12] apply a large number of patterns to the CUT that facilitate the detection of non-modeled faults; however, they may be unsuitable for use during short idle time durations or during system start-up.

In this paper, we propose a deterministic test-per-scan BIST architecture that is fully autonomous and suitable for field testing. A small set of test patterns that provides complete detectable stuck-at fault coverage is applied to the CUT. Such short test sequences are very useful for testing systems during startup, idle states or shutdown. They also ensure a low error detection latency, which is highly desirable for safety-critical applications. This approach obviates the need for storing multiple seeds for BIST since the test generation logic is hard-wired into the system. We exploit recent research in automatic test pattern generation methods, which has led to techniques and tools that provide compact test sets for large combinational and scan-based circuits [7]. We synthesize the BIST logic for field testing for several ISCAS 89 benchmarks and two industrial circuit modules and show that the BIST overhead is low in all cases. Deterministic BIST has been widely assumed to be too expensive; our results however show that low-cost deterministic BIST can often be used for efficient field testing of high-availability systems.

We also present a mixed-mode BIST strategy in which pseudorandom patterns are fed into the scan chain whenever longer idle time durations are available for field testing. Since deterministic testing is necessary only for the random-pattern-resistant faults, this approach reduces the size of the precomputed test set and lowers the overall overhead for BIST.

The paper is organized as follows. Section 2 discusses the proposed test architecture and some of its variants. Section 3 presents experimental results for some representative circuits. Finally, we present our conclusions in Section 4.

## 2 BIST Architecture

As discussed in section 1, a conventional scan-BIST architecture uses an LFSR to generate pseudo-random patterns that are serially loaded into each scan chain of the circuit under

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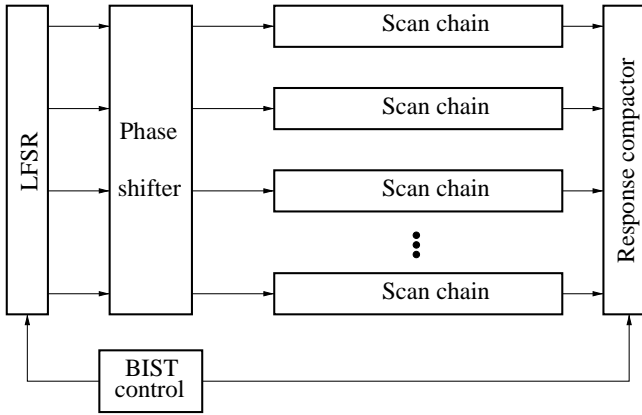


Figure 1: A typical BIST architecture based on pseudorandom patterns.

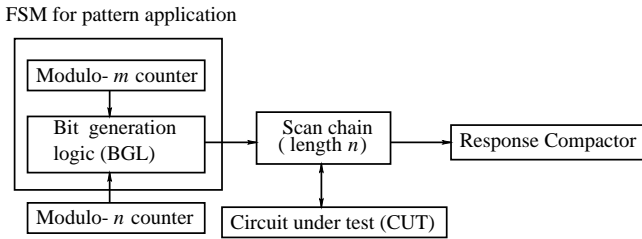


Figure 2: Proposed deterministic scan-BIST architecture.

test (Figure 1). The test responses are transferred to the scan chain, and the scan out process is overlapped with the scan-in of the next test pattern. A scan-BIST architecture requires low hardware overhead and is useful for circuits that are random-pattern testable. However, most realistic circuits have a large number of random-pattern-resistant faults; long sequences of pseudorandom patterns are required for these circuits in order to achieve acceptable fault coverage. The application of long test sequences takes a large amount of time, which limits the use of pseudorandom scan-BIST methods for field testing. While phase shifters and test points [3] increase fault coverage, the testing time is still too high for high-availability systems that must be tested during very short idle periods.

We propose a deterministic scan-BIST architecture in which a small set  $T_D$  of precomputed deterministic patterns that provides complete fault coverage is applied to the CUT during field testing. The overall test architecture for a single scan chain is shown in Figure 2. (The design can be easily extended to multiple scan chains.) The bits of  $T_D$  are fed into the scan chain using a special bit generation logic (BGL) block. In addition to the BGL block, two binary counters are used for pattern application. These counters are of size  $\lceil \log_2 m \rceil$  and  $\lceil \log_2 n \rceil$  bits, respectively, where  $T_D$  contains  $m$  patterns and the scan chain is of length  $n$ . Note that the  $\lceil \log_2 n \rceil$ -bit counter, which we refer to as the position counter, is part of the BIST controller for any autonomous BIST scheme [8]. In

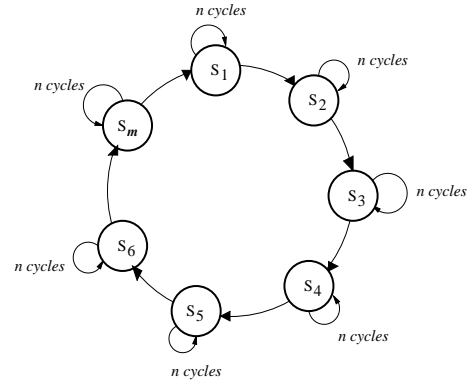


Figure 3: State transition diagram of the finite-state machine used for delivering test patterns during field testing.

the following discussion, we refer to the  $\lceil \log_2 m \rceil$ -bit counter as the pattern counter. A similar scheme based on the use of the BIST control logic was presented in [12]; however, it is applicable only to the embedding of deterministic patterns in long pseudorandom sequences generated by an LFSR.

While the logical separation between the pattern counter and the BGL block is useful for understanding the BIST architecture, it is more convenient to merge the pattern counter with the BGL block and view the combined finite-state machine (FSM) as the vehicle for pattern delivery. This FSM can be easily synthesized using CAD tools. We use Synopsys Design Compiler [9] for synthesis in our work.

Figure 3 illustrates the state diagram of the FSM for pattern generation. This Mealy-type FSM has  $m$  states, each state corresponding to a test pattern in  $T_D$ . It is fed by the  $\lceil \log_2 n \rceil$  outputs from the modulo- $n$  position counter. We assume that the position counter, which is used for BIST control, behaves as a binary counter whose states appear in a normal binary sequence. Since the patterns in  $T_D$  can be reordered without affecting fault coverage, the states  $S_1, S_2, S_3, \dots, S_m$  of the FSM can be specified symbolically. Thus, even though a test pattern  $t_i \in T_D$  is mapped to state  $S_i$ ,  $1 \leq i \leq m$ , the actual order of application of the patterns is determined by the synthesis tool.

The FSM of Figure 3 operates as follows :

1. It is initially in the state  $S_1$  corresponding to the first test pattern  $t_1$  in  $T_D$ . The  $n$  bits of  $t_1$  are serially loaded into the scan chain in  $n$  scan cycles.
2. After  $n$  cycles, the test responses are captured using the functional clock, and the FSM goes to the state  $S_2$  corresponding to the second test pattern  $t_2$  in  $T_D$ . The  $n$  bits of  $t_2$  are then serially loaded into the scan chain, while the test response for  $t_1$  is scanned out.
3. This process continues until all the test patterns have been scanned in and the test responses captured in the scan chain.

A limitation of the proposed BIST architecture is that it is

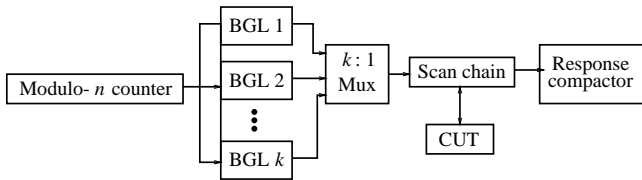


Figure 4: Modified deterministic test-per-scan BIST architecture.

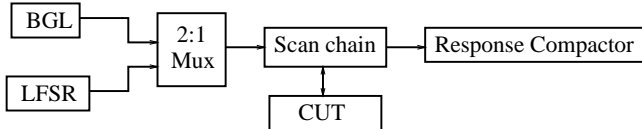


Figure 5: Mixed-mode BIST architecture.

inefficient (hardware overhead is high) if  $T_D$  contains a large number of patterns. In these cases, we partition  $T_D$  and use the modified BIST architecture as shown in Figure 4. In this approach,  $T_D$  is partitioned into  $k$  smaller groups of  $m/k$  patterns. Therefore, there are  $k$  BIST circuits corresponding to the  $k$  groups. This architecture requires a  $k$ -to-1 multiplexer to switch between the BIST circuits. However, the area of a  $k$ -to-1 multiplexer is a very small fraction of the BIST logic area and hence does not increase the area overhead significantly. We then obtain the overall BIST logic area by adding the areas of the individual BIST subcircuits.

In order to further reduce the BIST overhead, a mixed-mode scheme can be used for test pattern application in situations when longer idle time durations are available for field testing. We first apply a large number (typically 1M) of pseudorandom patterns, so that random-pattern-testable faults and many non-modeled faults are detected. The deterministic test patterns for hard faults is then obtained by using a fault-oriented automatic test pattern generation program and the BIST logic is synthesized using the test set for the hard faults. The BIST architecture that we employ for mixed-mode operation is shown in Figure 5. The proposed BIST pattern generator hardware can be combined with any response monitor circuit, e.g, a sufficiently large LFSR, that generates a fault signature with a very low aliasing probability.

### 3 Experimental Results

In this section, we present experimental results on the synthesis of BIST logic for full-scan versions of several large ISCAS 89 benchmark circuits and two industrial circuit modules. We used compacted test sets obtained from the Mintest ATPG program developed at the University of Illinois [7] for our experiments with the ISCAS benchmarks. For the industrial circuits CKT1 and CKT2, the test sets were generated using the Mentor Graphics Fastscan tool. We carried out our experiments on a Sun Ultra-10 workstation with 128 MB of DRAM.

We carried out two sets of BIST synthesis experiments: (a)

A fully deterministic approach without pseudorandom patterns and (b) A mixed-mode approach with the application of upto 2 million pseudorandom patterns to the CUT. The results on BIST synthesis for the fully deterministic approach are shown in Table 1. We obtained the data on circuit area by mapping the CUT and the BIST logic to the Synopsys *lsi\_10K* library [9]. We include both gate and interconnect area in our overhead calculation. The BIST logic area refers to the area of the FSM of the Figure 3, which includes the bit generation logic merged with the pattern counter. The gate area figures are obtained from the cell areas in the *lsi\_10K* library, and the interconnect area figures are obtained by using realistic wire-load models.

We compare our results with a recent pseudorandom scan-BIST architecture [10], which uses multiple test sessions and a varying number of capture cycles after each scan-in. The latter increases testing time considerably and is therefore inherently unsuitable for field testing of high-availability systems. As shown in Table 2, we achieve higher fault coverage than that reported in [10] and [12] with a shorter test length. Although the hardware overhead values reported in [10] include the cost of the output data compactor, BIST controller and multiplexers, and are generally lower than in our method, they do not include the routing and interconnect area, which may be a high percentage of the total overhead. The method in [10] requires DFT techniques such as test-point insertion in order to achieve high fault coverage. No such intrusive DFT technique is required for our proposed scan-BIST method. We do not compare our hardware overhead with that of [12] since the latter only reports BIST area in  $\text{mm}^2$  units and it does not present any overhead data. We also do not present the results for the ISCAS 85 benchmark circuits in Table 1 since they do not have internal scan.

As discussed in Section 2, we use the partitioned BIST scheme for circuits whose test sets contain a large number of test patterns. In these cases, if partitioning is not used, the BIST synthesis problem exceeds the capacity of the Synopsys Design Compiler. For example, the BIST logic for the industrial circuit CKT2 was synthesized by partitioning the test set into 25 subsets. This requires a multiplexer to switch between several BIST sub-blocks; however its area is negligible compared to the other components of the BIST logic. Synthesizing such an FSM takes several hours of CPU time; however, it is only a one-time design, and represents a modest investment over the lifetime of the product.

For the mixed-mode approach, we used the FSIM fault simulator [11] for detecting random-pattern-testable faults using pseudorandom patterns. Fault-oriented ATPG was then performed using the Atalanta ATPG program [11] to obtain a small set of deterministic patterns for the hard-to-detect faults. Table 3 presents the results on BIST synthesis for the mixed-mode approach. We neglect the area of the LFSR in the calculation of the hardware overhead.

Table 1: Results on BIST synthesis for the fully deterministic approach.

Circuit	Length of scan chain $n$	Number of patterns $m$	Number of gates in the circuit	Circuit area ( $lsi\_10K$ units)	Area of BIST logic ( $lsi\_10K$ units)	Hardware Overhead (percent)	Hardware Overhead in [10] (percent)
s15850	611	94	3448	15839.0	1306.2	8.0	6.3
s35932	1763	12	12204	33345.0	286.7	0.9	2.4
s38417	1664	68	8709	38011.0	1141.9	3.0	2.0
s38584	1464	110	11448	37372.0	4570.1	12.2	1.9
CKT1	282	45	2176	7454.0	592.0	7.9	N/A
CKT2	862	371	25973	66000.0	5358.1	8.1	N/A

Table 2: Comparison of fault coverage between the proposed method and [10].

Circuit	Fault coverage of proposed method (%)	Fault coverage (no test points) in [10] (%)	Fault coverage in [12] (%)	Test length (cycles)	Test length in [10] (cycles)
s15850	100	87.19	97.25	57528	254337
s35932	100	89.02	N/A	21168	2850
s38417	100	91.82	93.62	113220	204400
s38584	100	93.51	98.93	161150	167187

Table 3: Results on BIST synthesis for the mixed mode approach.

Circuit	Length of scan chain ( $n$ )	Number of pseudorandom patterns	Number of deterministic patterns	Circuit area ( $lsi\_10K$ units)	Area of BIST logic ( $lsi\_10K$ units)	Hardware Overhead (percent)
s13207	700	64K	17	13973.0	169.0	1.0
s15850	611	1 M	65	15839.0	1120.1	7.1
s38417	1664	2 M	26	38011.0	706.2	1.9
s38584	1464	64K	50	37372.0	2250.3	6.0

## 4 Conclusions

We have presented a new deterministic scan-BIST architecture which allows a compact, precomputed test set, guaranteed to provide complete fault coverage, to be applied to the CUT during field testing. The proposed approach reduces both fault and error latency, and is especially suitable for high-availability systems with low downtimes.

The test patterns in the precomputed test set are generated using a dedicated finite-state machine. We have synthesized the BIST logic for several ISCAS 89 benchmarks and two industrial circuit modules. Since the BIST logic is hardwired into the system, there are no storage requirements for the test patterns. It has been shown that the hardware overhead required for the BIST logic is low in all cases. We have compared our results to those obtained in [10]. Although the method in [10] requires lower overhead (ignoring interconnect area), the fault coverage of our method is higher. Also, no modifications are required in the CUT in the proposed method.

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