Power Management Using Test-Pattern Ordering for Wafer-Level Test During Burn-In

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Abstract—Wafer-level test during burn-in (WLTBI) is a promising technique to reduce test and burn-in costs in semiconductor manufacturing. However, scan-based testing leads to significant power variations in a die during test-pattern application. This variation adversely affects the accuracy of predictions of junction temperatures and the time required for burn-in. We present a test-pattern ordering technique for WLTBI, where the objective is to minimize the variation in power consumption during test application. The test-pattern ordering problem for WLTBI is formulated and solved optimally using integer linear programming. Efficient heuristic methods are also presented to easily solve the pattern-ordering problem for large circuits. Simulation results are presented for the ISCAS'89 and the IWLS'05 benchmark circuits, and the proposed ordering technique is compared with two baseline methods that carry out pattern ordering to minimize peak power and average power, respectively. A third baseline method that randomly orders test patterns is also used to evaluate the proposed methods.

Index Terms—Wafer-level test during burn-in (WLTBI), test-pattern ordering, test power.

I. INTRODUCTION

MANUFACTURING test is a significant contributor to the product cost for deep-submicrometer ICs [1]. In addition to the need for effective test techniques for defect screening and speed binning for these ICs, there is an ever-increasing demand for high device reliability and low defective parts-per-million levels. Semiconductor manufacturers routinely perform reliability screening on all devices before shipping them to customers [2]. Accelerated test techniques shorten time-to-failure for defective parts without altering the device failure characteristics [3]. Burn-in is one such technique that is widely used in the semiconductor industry [3], [4].

The long time intervals associated with burn-in result in high cost [1], [5], [6]. It is, however, unlikely that burn-in will be completely eliminated in the near future for high-performance chips and microprocessors [1]. Wafer-level burn-in (WLBI) has recently emerged as an enabling technology to lower the cost of burn-in [4]. In this approach, devices are subjected to burn-in and electrical testing while in the bare wafer form. By moving

the burn-in process to the wafer level, significant cost savings can be achieved in the form of lower packaging costs, as well as reduced burn-in and test time.

In this paper, we address power-conscious test-pattern ordering for wafer-level test during burn-in (WLTBI). The solutions methods, which are based on integer linear programming (ILP) and efficient heuristics, allow us to determine an appropriate ordering of test patterns that minimizes the overall cycle-by-cycle variation in power. Reduced variance in test power results in less fluctuations in the junction temperatures of the device. It has been shown in [7] that the junction temperature of the die is a function of the ambient temperature, the device thermal resistance, and the power consumption of the device. Maintaining the spread in power consumption during test will therefore significantly lower the variations in junction temperature.

The key contributions of this paper are as follows.

- 1) We motivate the importance of handling thermal problems during WLTBI, and show how test-pattern ordering can be used to alleviate these problems.
- 2) We present a test-pattern ordering technique based on ILP for scan-based WLTBI. Our goal is to minimize the variations in the test power of the device during test application.
- 3) We develop a heuristic technique to solve the test pattern ordering problem for large circuits.
- 4) We also develop a second heuristic technique based on ILP for large circuits.

The remainder of the paper is organized as follows. Motivation and additional background for this paper are presented in Section II. Section III describes thermal challenges associated with WLTBI, and motivates the need for a test-pattern ordering approach that is tailored for WLTBI. Section IV presents an overview of cycle-accurate power modeling technique for scan-based circuits. It also presents the ILP-based test-pattern ordering technique for WLTBI. In Section V, two heuristic methods to solve the problem efficiently are presented. The baseline methods used to evaluate the test-pattern ordering techniques are presented in Section VI. Section VII presents simulation results for several ISCAS'89 and IWLS'05 benchmark circuits [8]. Finally, Section VIII concludes the paper.

II. MOTIVATION AND BACKGROUND

Test during burn-in at the wafer level enhances the benefits that are derived from the burn-in process. The monitoring of device responses while applying suitable test stimuli during WLBI leads to the easier identification of faulty devices.

We refer to this process as “WLTBI”; it is also referred to in the literature as “test in burn-in” (TIBI) [3], “wafer-level

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Fig. 1. Test and burn-in flow using. (a) PLBI. (b) WLTBI.

burn-in test” (WLBT) [9], etc. WLTBI technology has recently made rapid advances with the advent of the “known good die” (KGD) [10], i.e., devices that are sold as tested bare die. KGDs are building blocks of complex system-in-package (SiP) designs, where chips with different functionalities are combined in a single package. The growing demand for KGDs in complex system-on-a-chip (SoC)/SiP architectures, multichip modules, and stacked memories, highlights the importance for cost-effective and viable WLTBI solutions [4]. WLTBI will also facilitate advances in the manufacture of 3-D ICs, where bare dies or wafers must be tested before they are vertically stacked. WLTBI can therefore be viewed as an enabling technology for cost-efficient manufacture of reliable 3-D ICs.

Fig. 1 illustrates and compares the test and burn-in flow in a semiconductor manufacturing process. The manufacturing flow for package-level burn-in (PLBI) is shown in Fig. 1(a); Fig. 1(b) highlights the manufacturing flow when WLTBI is employed for test and burn-in at the wafer-level. Test and burn-in of devices in the bare wafer form can potentially reduce the need for post-packaging test and burn-in for packaged chips and KGDs. In the manufacture of KGDs, WLTBI eliminates the need for a die carrier and carrier burn-in, thereby resulting in significant cost savings.

The basic techniques used for the testing and burn-in of individual chips are the same as those used in WLTBI. Test and burn-in require the availability of suitable electrical excitation of the device/die under test (DUT), irrespective of whether it is

done on a packaged chip or a bare die. The only difference lies in the mode of delivery of the electrical excitation. Mechanically contacting the leads provides electrical bias and excitation during conventional testing and burn-in. In the case of WLTBI, this excitation can be provided in any of the following three ways: the probe-per-pad method, the sacrificial metal method, and the built-in test/burn-in method [11].

The built-in test/burn-in method involves the use of on-chip design-for-test (DfT) infrastructure to achieve WLTBI. This technique allows wafers to undergo full-wafer contact using far fewer probe contacts. The presence of sophisticated built-in DfT features on modern day ICs makes “monitored burn-in” possible. *Monitored burn-in* is a process where a DUT is provided with input test patterns; the output responses of the DUT are monitored online, thereby leading to the identification of failing devices. It is therefore clear that WLTBI has a significant potential to lower the overall product cost by breaking the barrier between burn-in and test processes. As a result, ATE manufacturers have recently introduced WLTBI and test equipment that provide full-wafer contact during burn-in and also provide test monitoring capabilities [4], [9], [12].

There are several practical challenges associated with WLTBI; these include full contact burn-in and efficient thermal control [11]. Successful WLTBI operation also requires thorough understanding of the thermal characteristics of the DUT. In order to keep the burn-in time to a minimum, it is essential to test the devices at the upper end of their temperature envelope

[7]. Moreover, the junction temperatures of the DUT need to be maintained within a small window such that burn-in predictions are accurate.

Power management for WLTBI is especially important for scan testing. Scan-based testing is now widely used in the semiconductor industry [13]. However, scan testing leads to complex power profiles during test application; in particular, there is a significant variation in the power consumption of a device under test on a cycle-by-cycle basis. In a burn-in environment, the high variance in scan power adversely affects predictions on burn-in time, resulting in a device being subjected to excessive or insufficient burn-in [14]. Incorrect predictions may also result in thermal runaway.

Dynamic burn-in using a full-scan circuit automatic test pattern generation (ATPG) was proposed in [15] with the objective of maximizing the number of transitions in the scan chains. The higher power consumption of ICs during scan-based testing is a serious concern in the semiconductor industry; scan power is often several times higher than the device power dissipation during normal circuit operation [16]. Excessive power consumption during scan testing can lead to yield loss. As a result, power minimization during test-pattern application has recently received much attention [17]–[22]. Research has focused on pattern ordering to reduce test power [17], [23], [24]. The pattern-ordering problem has been mapped to the well-known traveling salesman problem (TSP) [23], [24]. Testing semiconductor devices during burn-in at wafer-level requires low variation in power consumption during test [7]. A test-pattern re-ordering method that minimizes the dynamic power consumption does not address the needs of WLTBI. Specific techniques need to be developed to address this aspect of low-power testing, i.e., the ordering of test patterns to minimize the overall variation in power consumption.

III. THERMAL CHALLENGES DURING WLTBI

The challenges that are encountered during WLTBI are a combination of the problems faced during the sort process and during burn-in. Wafer sort is used to identify defective dies at wafer level before they are assembled in a package. It is also the first test-related step in the manufacturing process where thermal management plays an important role. Current wafer probers use a thermal chuck to control the device temperature during the sort process. The chuck is an actively regulated metal device controlled by external chillers and heaters embedded under the device [7]. The junction temperature of the DUT is determined by the following relationship [7], [25], [26]:

$$T_j = T_a + P\theta_{ja} \quad (1)$$

where T_j is the junction temperature of the device, T_a is the ambient temperature, P is the device power consumption, and θ_{ja} is the thermal resistance (junction to ambient) of the device. The value of T_j is therefore determined by the device power consumption, thermal resistance, and a constant T_a . The previous relationship has been derived in [26] using a first-order approximation of the electrical equivalent of the die and tester assembly. Even though each circuit block in the die has different activity (and temperature), latchup phenomenon occurs in some part of

Fig. 2. Thermal challenges involved in WLTBI.

the chip, and the local temperature increase rapidly spreads over the entire die and causes thermal breakdown [26]. It is therefore reasonable to assume a single value of T_j for the entire device.

The controllability of T_j is limited by the extent to which the parameters T_a and P can be controlled. Considerable power fluctuations during the test of the DUT can significantly affect the value of T_j for the DUT, thereby adversely impacting the reliability screening process. Fig. 2 illustrates a power profile of the die during burn-in. The time required for burn-in is predicted based on the median value of T_j [7]; this, in turn, is determined by the value of power dissipation P_{BI} shown in Fig. 2. When the power dissipation increases beyond P_{BI} , it results in the die being subject to over burn-in, which may result in yield loss and even thermal runaway. On the other hand, when the power dissipation is below P_{BI} , the die is subjected to under burn-in; this can result in the test escape of latent defects. One of the important goals of the burn-in process is to keep the burn-in time to a minimum, thereby increasing throughput, and minimizing equipment and processing costs. It is important to have a tight spread in temperature distribution of the device (by maintaining the power dissipation within an acceptable threshold) to increase yield and at the same time minimize burn-in time [7].

It is this issue of controlling the spread in T_j over the period of test application that we address in this paper. We use the test power of the DUT as a means to control T_j of the device. The problem of controlling the power profiles, which depend on the ordering of test patterns has been ignored so far in literature. We therefore develop a power-conscious test-pattern ordering approach, specifically suited for WLTBI.

IV. CYCLE-ACCURATE TEST POWER MODELING AND TEST-PATTERN ORDERING PROBLEM

In this section, we first review cycle-accurate test power modeling and the method used to estimate test power. We next describe the test-pattern ordering problem. A solution method based on ILP is also presented. In this paper, we consider that the test patterns are fully specified. If the test patterns contain don't care (X) bits, WLTBI-specific X -fill techniques [27] can be used prior to pattern ordering.

A. Background

A significant percentage of scan cells change values in every scan shift and scan capture cycle. The toggling of scan flip-flops can result in excessive switching activity during test, resulting in high power consumption. It has been shown in [19] that the number of transitions of the DUT is proportional to the number

Fig. 3. Example to illustrate scan shift operation.

of transitions in the device scan chains. Therefore, a reduction in the number of transitions in the scan cells during test application leads to lower test power. A number of techniques have been developed to reduce the peak power and average power consumption during test by reducing the number of transitions in the scan chain [18], [28]. These techniques rely on test-pattern ordering [29]–[32], scan chain ordering [23], [33], [34], and the use of multiple capture cycles during test application [29] to reduce the toggling of scan cells during shift/capture cycles. Segmented scan approaches [20], [21], [35] have also been used to address test power issues for industrial designs.

B. Scan-Chain Transition-Count Calculation

A metric known as the weighted transition count (WTC) was presented in [19] to calculate the number of transitions in the scan chain during scan shifting. It was also shown in [19] that the WTC has a strong correlation with the total device consumption. The WTC metric can be extended easily to determine the cycle-by-cycle transition counts while applying test patterns. The knowledge of the length of the scan chains, the test pattern to be scanned in, and the initial state of the scan cells (response from previously applied test stimulus) can be used to generate cycle-accurate test power data.

We next illustrate the procedure to determine cycle-accurate power consumption. Let us consider the case of a circuit under test (CUT) with six scan cells $FF_1, FF_2, FF_3, FF_4, FF_5, FF_6$, and a test pattern $tp = (110110)$ being scanned in. Let the initial state of scan cells be $tr = (101110)$. Fig. 3 represents the cycle-by-cycle change in the values of the scan cells when the test pattern is scanned in, and the test response is scanned out. The scan-in and scan-out of the test pattern and responses are not the only contributors to the change in values of the scan cells. It is also important to consider the transitions that occur during the capture cycle. The number of transitions that occur during the capture cycle can be calculated by determining the Hamming distance between the test stimuli and its expected test response.

Let us consider a scan chain of length n that has an initial value $ti = (ti_1, \dots, ti_n)$, and a test pattern $tp = (tp_1, \dots, tp_n)$ that is shifted into the scan chain. The transitions that occur during the shifting of the test pattern (and shifting out the previous state test response) can be represented as an $n \times n$ matrix T [36]. An element t_{ij} of T is 1 if there is a transition in scan cell j during clock cycle i , otherwise, $t_{ij} = 0$. The parameter T can be used to calculate the total number of scan cell transitions (a measure of the power consumption during test) during every

clock cycle. During any given clock cycle i , the total number of transitions $tr(i)$ can be calculated by summing the values of all elements in row i of T ; this can be expressed using the equation $tr(i) = \sum_{j=1}^n t_{ij}$.

For the example shown in Fig. 3, the cycle-by-cycle number of scan cell transitions is given by the set $\{4, 4, 4, 4, 5, 4\}$. For the test response (111100), the number of transitions that occur during the capture cycle for this example is 2. For multiple scan chains, the aforementioned calculation can simply be carried out independently for each scan chain.

C. Test-Pattern Ordering Problem: $\mathcal{P}_{TPO}$

We next present the test-pattern ordering problem $\mathcal{P}_{TPO}$. The goal is to determine an optimal ordering of test patterns for scan-based testing, such that the overall variation in power consumption during test is minimized. For simplicity of discussion, we assume a single scan chain for test application and N patterns $T_1, T_2, \dots, T_N$. The extension of $\mathcal{P}_{TPO}$ to a circuit with multiple scan chains is trivial. The test application for the CUT is carried out as follows.

- 1) The scan flip-flops in the circuit are all assumed to be initialized to 0.
- 2) The test application procedure is initiated by shifting in the first test pattern into the circuit.
- 3) The scan-out of the first test response and the scan-in of the next pattern are then carried out simultaneously. This process is repeated until all the test patterns are applied to the CUT, and all test responses are shifted out of the circuit.
- 4) The scan-out of the final test response terminates the test application process for the CUT.

We next compute the cycle-by-cycle power when response R_i is shifted out and test pattern T_j is shifted in, for a scan chain of length n . Let $TC_k(R_i, T_j), 1 \leq k \leq n$, denote the power (number of transitions) for shift cycle k . The overall test power can be represented by the following set $TC(R_i, T_j) = \{TC_1(R_i, T_j), \dots, TC_n(R_i, T_j), TC_{n+1}(R_i, T_j)\}$. The parameter $TC_{n+1}(R_i, T_j)$ denotes the number of transitions during the capture cycle. The average power consumption for $TC(R_i, T_j), \mu(R_i, T_j)$ is given by $(\sum_{k=1}^{n+1} TC_k(R_i, T_j)) / (n+1)$. The statistical variance in test power $\sigma^2(R_i, T_j)$ is given by

$$\sigma^2(R_i, T_j) = 1/n \sum_{k=1}^{n+1} (TC_k(R_i, T_j) - \mu(R_i, T_j))^2.$$

For the example in Fig. 3, the average power consumption and the statistical variance in test power are 3.85 and 0.80, respectively. We use the following two measures as metrics to analyze the variation in power consumption.

- 1) The first measure is the statistical variance in test power consumption. Let T_{tot} be the test time (in clock cycles) needed to apply all the test patterns for the CUT. Let P_{mean} be the mean value of power consumption per clock cycle during test. The variance in test power consumption for the CUT is defined as $(1)/(T_{tot} - 1) \sum_{i=1}^{T_{tot}} (P_i - P_{mean})^2$. Low variance indicates low (aggregated) deviation in test power from the mean value of power consumption during test. Successful WLTBI requires the minimization of this metric.

- 2) The total cycle-to-cycle variation in test power consumption is an indicator of the “flatness” of the power profile during test. Large cycle-to-cycle power variations are undesirable. We therefore quantify the “flatness” of the power profile using a measure T_{th} , obtained by counting the number of clock cycles i for which $(|P_i - P_{i+1}|)/(P_i)$ exceeds a threshold γ . The parameter P_i denotes the power consumption during the i th clock cycle. A large value of T_{th} for a given value of γ is undesirable for WLTBI.

The optimization problem $\mathcal{P}_{TPO}$ can now be formally stated as follows.

$\mathcal{P}_{TPO}$: Given a CUT with test set $T = \{T_1, T_2, \dots, T_N\}$, determine an optimal ordering of test patterns such that: 1) the overall variation in power consumption during test is minimized and 2) the constraint on peak power consumption P_{max} during test is satisfied. As a preprocessing step, the cycle-accurate power information for all pairs of patterns and $\sigma^2(R_i, T_j) \forall i, j$ need to be computed. For N test patterns, with scan chains of length n , this step takes $O(nN^2)$ time.

A binary indicator variable $x_{ij}, S \leq i \leq N, 1 \leq j \leq E$, is used in the optimization problem to ensure that each test pattern appears exactly once in the ordered sequence. It is defined as follows:

$$x_{ij} = \begin{cases} 1, & \text{if } T_j \text{ immediately follows } T_i \\ 0, & \text{otherwise.} \end{cases}$$

We use S to denote a (dummy) start pattern and $x_{iS} = 0 \forall i \Rightarrow 1 \leq i \leq N$. Likewise, E denotes a (dummy) end pattern and $x_{Ei} = 0 \forall i \Rightarrow 1 \leq i \leq N$.

The objective function for the optimization problem can be written as follows:

$$\text{Minimize } \mathcal{F} = \max_{\forall i} \left\{ \sum_{j=1}^N x_{ij} \sigma^2(R_i, T_j) \right\}.$$

We use a min-max objective function for the test-pattern ordering problem in order to minimize the variance in test power between any two consecutive test patterns. The “max” function identifies, among all pairs of consecutive patterns, the pattern-pair that leads to the highest power variance. Therefore, this model and the resulting solution results in an ordering of test patterns where the maximum variance in test power for any two consecutive patterns is minimum.

The aforementioned min-max objective function can be linearized as follows:

$$\text{Minimize } \mathcal{C}, \text{ subject to } \mathcal{C} \geq \sum_{j=1}^N x_{ij} \sigma^2(R_i, T_j), \quad 1 \leq i \leq N.$$

Next we formulate constraints to ensure that a test pattern is followed (and preceded) by exactly one pattern. This constraint can be represented by the following two sets of equations:

$$\begin{aligned} \sum_{j=1}^N x_{ij} &= 1, & i &= S, 1, 2, \dots, N \\ \sum_{i=1}^N x_{ij} &= 1, & j &= 1, 2, \dots, E. \end{aligned}$$

Minimize $\mathcal{C}$, subject to :

- 1) $\mathcal{C} \geq \left\{ \sum_{j=1}^N x_{ij} \cdot \sigma^2(R_i, T_j) \right\} \forall i$
- 2) $\sum_{j=1}^N x_{ij} = 1, i = S, 1, 2, \dots, N$
- 3) $\sum_{i=1}^N x_{ij} = 1, j = 1, 2, \dots, E$
- 4) $x_{i,S} = 0, \forall i$
- 5) $x_{E,i} = 0, \forall i$
- 6) $x_{ij} = 0$ if $\max\{TC(R_i, T_j)\} > P_{max}$
- 7) $\frac{|TC_n(R_i, T_j) - TC_1(R_j, T_k)|}{TC_n(R_i, T_j)} > TC_{th} \Rightarrow u_{ijk} = 0$
- 8) $x_{ij} + x_{jk} \leq u_{ijk} + 1$
- 9) $x_{ij} + x_{jk} \geq 2u_{ijk}$

/* Constants : $TC_{th}, P_{max}, N, \sigma^2(R_i, T_j), \max\{TC(R_i, T_j)\} *$

/* Variables : $u_{ijk}, x_{ij}, x_{jk} *$

Fig. 4. ILP model for $\mathcal{P}_{TPO}$.

We next formulate constraints imposed by the upper limit on peak power consumption during any given clock cycle. Let us assume that the maximum constraint on peak power consumption at any given clock cycle is P_{max} ; the constraint to ensure that this limit on power consumption is never violated can be written as

$$x_{ij} = 0, \quad \text{if } \max\{TC(R_i, T_j)\} > P_{max}.$$

Thus far, the model does not consider the change in power consumption when test response R_i of test pattern T_i is scanned out, and two test patterns T_j, T_k are applied consecutively. It is important during WLTBI to ensure that the power consumption between any two consecutive test patterns does not change dramatically. We therefore need to maintain the change in test power between two consecutive patterns within a reasonable threshold TC_{th} . This value is chosen starting with the lowest value of TC_{th} necessary to formulate a valid ordering. We model this constraint as follows:

$$\frac{|TC_n(R_i, T_j) - TC_1(R_j, T_k)|}{TC_n(R_i, T_j)} > TC_{th} \Rightarrow x_{ij}x_{jk} = 0.$$

The term $|TC_n(R_i, T_j) - TC_1(R_j, T_k)|$ reflects the change in transition count between T_j and T_k . This change is expressed as a fraction of transition count for the last shift cycle of T_j . The $x_{ij}x_{jk}$ product term is nonlinear and it can be replaced with a new binary variable u_{ijk} and two additional constraints

$$\begin{aligned} x_{ij} + x_{jk} &\leq u_{ijk} + 1 \\ x_{ij} + x_{jk} &\geq 2u_{ijk}. \end{aligned}$$

In the worst case, the number of variables in the previous ILP model is $O(N^3)$ and the number of constraints is also $O(N^3)$. The complete ILP model is shown in Fig. 4.

D. Computational Complexity of $\mathcal{P}_{TPO}$

It can be easily shown that the pattern-ordering problem for WLTBI is NP-complete. The objective of $\mathcal{P}_{TPO}$ is to determine an ordering of the N test patterns $\langle O_1, O_2, \dots, O_N \rangle$ that minimizes $\max\{\sigma^2(R_{O_1}, T_{O_2}), \sigma^2(R_{O_2}, T_{O_3}), \dots, \sigma^2(R_{O_{N-1}}, T_{O_N})\}$. Before we prove that the pattern-ordering problem for WLTBI

is NP-complete, we introduce the bottleneck TSP (BTSP) [37]. Consider a set $\{C_1, C_2, \dots, C_n\}$ of n cities. The problem of finding a tour that visits each city exactly once and minimizes the total distance traveled is known as TSP. In BTSP, we attempt to find a tour that minimizes the maximum distance traveled between any two adjacent cities in the tour. It has been shown in [37] that BTSP is NP-complete.

Claim: The pattern-ordering problem $\mathcal{P}_{\text{TPO}}$ is NP-complete.

Proof: We know that pattern-ordering problem is in NP because we can verify any solution in polynomial time with a simple $O(N^2)$ examination of all possible pattern combinations for ordering at each instant.

Let $G = (V, E)$ be a complete graph, where $V = \{C_1, \dots, C_n\}$ is the set of vertices and $E = \{(C_i, C_j) : C_i \neq C_j\}$ is the set of edges. Every edge (C_i, C_j) has an associated weight $w(i, j)$. In the BTSP context, a vertex can be interpreted as a city and the edge weight can be the distance between the cities or the time of travel between the two cities. With these notations, the BTSP problem is to find a tour that minimizes the maximum distance between any two cities in the tour.

The notations for the same graph $G = (V, E)$ can be written in the context of the pattern-ordering problem. In the context of the pattern-ordering problem, a vertex can be interpreted as a test pattern and the edge weight $w(i, j)$ can be used to represent $\sigma^2(R_i, T_j)$, i.e., variation in test power when test response i is scanned out while scanning in test pattern j .

An optimal ordering of test patterns is one that minimizes the maximum value of $\sigma^2(R_i, T_j)$. This is an exact instance of BTSP. An optimal ordering of test patterns that minimizes the maximum value of variation in test power consumption can be found in polynomial time if and only if a tour that minimizes the maximum distance between all two cities in the tour is found in polynomial time. This proves that $\mathcal{P}_{\text{TPO}}$ is NP-hard. Since $\mathcal{P}_{\text{TPO}}$ is in NP, we conclude that it is NP-complete. We next present a heuristic technique to solve $\mathcal{P}_{\text{TPO}}$ for large problem instances.

V. HEURISTIC METHODS FOR TEST-PATTERN ORDERING

The exact optimization procedure based on ILP is feasible only when the number of patterns is less than an upper limit, which depends on the CPU and the amount of available memory. To handle large problem instances, we present a heuristic approach to determine an ordering of test patterns for WLTBI, given the upper limit P_{max} on peak power consumption. The heuristic method consists of a sequence of four procedures. Its objective is similar to that of the ILP technique, i.e., to minimize the overall variation in power consumption during test. We start by determining cycle-accurate test power information for all pairs of test patterns in $O(nN^2)$ time. We next determine the first pattern to be shifted in, and then iteratively determine the ordering of patterns such that the variation in test power is minimized. The main steps used in the Pattern_Order heuristic, as shown in Fig. 5, are outlined next.

- 1) In procedure *Power_Determine*, the cycle-accurate information on test power consumption $TC(R_i, T_j)$ is determined for all possible pairs (R_i, T_j) .

Algorithm 1 *Pattern_Order*: Test-pattern ordering for WLTBI

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1: Let  $\sigma^2(R_i, T_j)$  be the standard deviation in test power when
   response  $R_i$  is scanned out and  $T_j$  is scanned in;
2: Let  $P_{\text{max}}$  be the constraint on peak power consumption;
3: Let  $N_{\text{pat}}$  be the total number of test patterns to be applied;
4: /*Procedure Power_Determine*/
5: for  $i = 1$  to  $N_{\text{pat}}$  do
6:   for  $j = 1$  to  $E$  do
7:     determine cycle-by-cycle power when test response  $R_j$  is
       scanned-out, and test pattern  $T_i$  is scanned-in;
8:     determine  $\sigma^2(R_j, T_i)$ ;
9:     determine  $P_{\text{max}}(R_j, T_i)$ ;
10:   end for
11: end for
12: /*Procedure Initial_Assign*/
13:  $\text{Length} = N_{\text{pat}}$ 
14:  $\text{min}_{\text{var}} = \infty$ ;
15: for  $i = 1$  to  $\text{Length}$  do
16:   if  $(\sigma^2(S, T_i) < \text{min}_{\text{var}}) \ \&\& \ (\max\{TC(S, T_i)\} < P_{\text{max}})$ 
     then
17:      $\text{min}_{\text{var}} = \sigma^2(S, T_i)$ ;
18:      $\text{Init}_{\text{pat}} = i$ ;
19:   end if
20: end for
21: first pattern to be ordered =  $\text{Init}_{\text{pat}}$ ;
22:  $\text{Length} = N_{\text{pat}} - 1$ 
23: /*Procedure Pat_Order*/
24: repeat
25:   for  $i = 1$  to  $\text{Length}$  do
26:     if  $(\sigma^2(\text{Init}_{\text{pat}}, \text{Length}(i)) < \text{min}_{\text{var}}) \ \&\& \ (\max\{TC(\text{Init}_{\text{pat}}, \text{Length}(i))\} < P_{\text{max}})$ 
       then
27:        $\text{min}_{\text{var}} = \sigma^2(\text{Init}_{\text{pat}}, \text{Length}(i))$ ;
28:        $\text{Init}_{\text{pat}} = \text{Unordered}(i)$ ;
29:     end if
30:   end for
31:    $\text{Length} = \text{Length} - 1$ ;
32:   Update list of unassigned patterns;
33: until  $\text{Length} = 0$ ;
34: /*Procedure Final_Assign*/
35: Last reordered pattern =  $\text{Unordered}(i)$ ;
36: Construct final ordered list of patterns for WLTBI.
```

Fig. 5. Pseudocode for the Pattern_Order heuristic.

- 2) In procedure *Initial_Assign*, the first test pattern to be shifted into the circuit is determined. The pattern T_i that yields the lowest value in test power variance $\sigma(S, T_i)$ is chosen as the first test pattern to be applied. We ensure that the constraint on peak power consumption P_{max} is not violated when T_i is applied to the CUT. The first pattern T_i that is added to the ordered list of test patterns is referred to as Init_{pat} .
- 3) In procedure *Pat_Order*, the subsequent ordering of patterns is iteratively determined. Once Init_{pat} is determined, the subsequent ordering of patterns are then iteratively determined by choosing the test pattern that results in the lowest test power variance $\sigma(\text{Init}_{\text{pat}}, T_i)$ without violating P_{max} .
- 4) In procedure *Final_Assign*, the lone unassigned test pattern is added last to the test ordering. A final list of ordered patterns for WLTBI can now be constructed using information from the *Initial_Assign* and the *Pat_Order* procedures.

A search operation is performed each time procedures *Initial_Assign* and *Pat_Order* are executed to determine the test pattern to be ordered. Hence, the worst-case computational complexity of the heuristic procedure, not including the $O(nN^2)$ initialization step, is $O(N \log_2 N)$.

Fig. 6. Impact of TC_{th} on test power variation for s5378. (a) $P_{max} = 145$. (b) $P_{max} = 150$.

TABLE I
PERCENTAGE REDUCTION IN THE VARIANCE OF TEST POWER CONSUMPTION OBTAINED USING ILP AND THE Pattern_Order HEURISTIC

Circuit	N	n	P_{max}	ILP						Pattern_Order					
				Baseline 1		Baseline 2		Baseline 3		Baseline 1		Baseline 2		Baseline 3	
				δV_{B1}	$\delta T_{th_{B1}}$	δV_{B2}	$\delta T_{th_{B2}}$	δV_{B3}	$\delta T_{th_{B3}}$	δV_{B1}	$\delta T_{th_{B1}}$	δV_{B2}	$\delta T_{th_{B2}}$	δV_{B3}	$\delta T_{th_{B3}}$
s1423	94	98	60	13.80	13.73	12.39	17.84	12.86	12.13	10.57	11.60	10.03	14.11	11.12	10.64
			65	11.12	11.39	10.21	14.10	10.79	10.48	8.73	9.08	7.91	11.62	7.53	7.06
s5378	155	313	145	12.07	9.02	10.47	9.02	13.14	12.60	8.63	8.91	7.42	6.03	8.15	7.87
			150	11.08	5.04	8.66	6.51	11.91	11.28	7.01	5.00	5.72	5.86	7.56	7.01
s35392	66	2083	1080	10.53	11.57	7.13	6.42	10.88	10.12	6.57	7.36	5.40	6.91	6.07	5.74
			1120	8.64	7.40	6.94	9.15	7.23	6.86	5.32	4.06	4.19	5.11	5.57	5.13
ac97_ctrl	106	2252	1210	9.13	10.32	6.88	7.21	11.12	11.64	7.91	8.10	6.49	7.33	9.87	10.23
			1220	6.93	6.97	6.08	6.37	8.04	8.63	6.15	6.58	5.79	5.90	7.61	8.11
			1230	6.91	6.94	6.07	6.33	8.00	8.58	6.09	6.52	5.71	5.88	7.56	7.97

A. ILP-Based Heuristic Method for Test-Pattern Ordering

A second heuristic method based on the ILP model for $\mathcal{P}_{TPO}$ can also be used to determine an ordering of patterns for WLTBI. The computational complexity associated with the ordering of a large number of test patterns limits the use of the ILP model for large circuits. Using a divide-and-conquer approach, the ILP model can recursively be applied to two or more subsets of test patterns for a circuit with large N . The ordered subsets of patterns can then be combined, by placing subsets that result in minimum cycle-to-cycle variation in power consumption adjacent to each other.

VI. BASELINE APPROACHES

In order to establish the effectiveness of the optimization framework for WLTBI, we consider three baseline methods. The first baseline method finds an ordering of test patterns that minimizes the average power consumption during test. The second baseline method finds an ordering of test patterns to minimize the peak power consumption during test. The third baseline randomly orders the test patterns.

A. Baseline Method 1: Average Power Consumption

The first baseline method determines an ordering of test patterns to minimize the average power consumption during test. The problem of reordering test sets to minimize average power has been addressed using the well-known TSP [23], [24]. Starting with the initial state S , consecutive test patterns are selected at each instance to minimize the average power consumption while not exceeding the constraint on peak power consumption P_{max} .

The aforementioned problem can be easily shown to be NP-hard [38]. Efficient heuristics are therefore necessary to determine an ordering of test patterns to minimize the average power consumption in a reasonable amount of CPU time. We use a heuristic technique based on the cross-entropy method [39]. The average power values are collected in a matrix of size $N \times N$. Each element in the matrix corresponds to an average power value for an ordered pair of patterns; for example, element (1, 2) in the matrix corresponds to the average power consumption when test pattern 2 is shifted in after test pattern 1. The heuristic technique takes the complete $N \times N$ matrix as an input to determine an ordering of test patterns.

B. Baseline Method 2: Peak Power Consumption

The second baseline approach determines an ordering of test patterns such that the peak power consumption is minimized during test. The objective function for this baseline method is as follows:

$$\text{Minimize } \mathcal{F} = \max_{1 \leq i \leq N} \left\{ \sum_{j=1}^N x_{ij} \mathcal{P}(R_i, T_j) \right\}$$

where $\mathcal{P}(R_i, T_j)$ denotes the peak power consumption when response R_i is shifted out while simultaneously shifting in T_j . This optimization problem can be easily solved to obtain a test-pattern ordering that reduces the peak power consumption. As in the case of $\mathcal{P}_{TPO}$, an ILP method can be used for this baseline for small problem instances. For large problem sizes, procedures Initial_Assign and Pat_Order can be modified to select a test-pattern ordering that results in the lowest peak power consumption.

TABLE II
PERCENTAGE REDUCTION IN THE VARIANCE OF TEST POWER CONSUMPTION OBTAINED
USING THE Pattern_Order HEURISTIC FOR SELECTED ISCAS'89 BENCHMARK CIRCUITS

Circuit	N	n	No. of scan chains	P_{max}	Baseline 1		Baseline 2		Baseline 3				
					δV_{B1}	$\delta T_{th_{B1}}$	δV_{B2}	$\delta T_{th_{B2}}$	δV_{B3}	$\delta T_{th_{B3}}$			
s9234	231	290	1	155	18.50	18.61	12.49	14.13	18.51	19.43			
				165	14.16	16.42	10.46	11.21	11.13	12.62			
				175	9.54	18.83	6.68	7.57	5.42	5.91			
			4	155	16.98	14.39	10.97	9.68	8.62	9.51			
				165	7.66	11.13	7.58	8.72	6.33	7.14			
				175	5.14	8.92	4.41	5.19	4.02	4.39			
			8	155	10.92	13.33	2.60	2.93	7.90	8.17			
				165	4.83	9.69	0.91	1.44	4.52	4.75			
				175	3.49	6.87	0.41	1.02	3.66	4.13			
s13207	311	723	1	460	4.43	5.11	1.12	4.00	4.59	4.72			
				470	2.90	3.58	0.97	1.88	3.12	3.37			
				480	2.89	3.58	0.97	1.88	3.12	3.37			
			4	460	3.56	3.94	0.78	3.24	3.73	4.02			
				470	2.19	2.74	0.41	0.61	2.53	2.81			
				480	2.19	2.73	0.41	0.61	2.53	2.81			
			8	470	1.81	1.62	0.26	1.31	1.99	2.11			
				480	1.81	1.62	0.26	1.31	1.99	2.11			
			s15850	210	761	1	400	16.66	25.71	10.57	14.33	14.71	17.54
410	11.19	19.19					6.96	8.05	9.42	11.17			
420	8.42	16.11					3.93	3.96	7.11	8.30			
4	410	8.22				14.34	4.95	5.19	6.31	7.02			
	420	4.94				9.13	0.14	0.09	5.16	5.93			
8	410	6.33				10.23	3.22	3.17	4.88	5.26			
	420	3.75				7.81	≈ 0	0.03	3.64	4.00			
s38417	198	764				1	390	4.08	6.39	3.39	3.62	2.59	2.82
							405	3.48	3.56	2.44	2.11	1.67	1.79
			415	0.77	0.81		0.25	0.40	0.08	0.15			
			4	405	3.06	3.42	2.16	3.53	1.80	1.94			
				415	0.54	0.67	0.09	0.28	≈ 0	0.06			
				s38584	162	1372	1	695	7.11	4.13	5.94	3.26	8.39
710	5.76	3.32	4.19					3.55	6.08	5.64			
720	3.51	2.86	2.84					1.92	4.70	3.98			
4	695	5.83	5.01				4.64	3.91	6.14	5.72			
	710	4.46	3.59				3.63	3.04	5.22	4.60			
	720	3.49	2.88				2.21	1.64	3.98	3.52			
8	695	3.21	2.61				2.52	2.03	3.68	3.17			
	710	2.20	1.75				1.43	1.08	2.76	2.21			

VII. EXPERIMENTAL RESULTS

In this section, we present experimental results for eight circuits from the ISCAS'89 test benchmarks, and IWLS'05 circuits. Since the objective of the test-pattern ordering problem is to minimize the variation in test power consumption during WLTBI, we present the following results.

- 1) The percentage difference in variance between baseline method 1 and the Pattern_Order heuristic. This difference is denoted by δV_{B1} , and it is computed as $(V_{Baseline1} - V_{Pattern_Order}) / (V_{Baseline1}) \times 100\%$; $V_{Pattern_Order}$ represents the variance in test power consumption obtained using the Pattern_Order heuristic, and $V_{Baseline1}$ represents the variance in power consumption obtained using the second baseline method.
- 2) The percentage difference in variance between baseline method 2 and the Pattern_Order heuristic. This is calculated in a similar fashion as $\delta V_{Baseline1}$, and is denoted as δV_{B2} .
- 3) The percentage difference in variance obtained using random ordering of test patterns and the Pattern_Order

heuristic. This is calculated in a similar fashion as $\delta V_{Baseline1}$, and is denoted as δV_{B3} .

- 4) We highlight the difference in the total number of clock cycles i during which $(|P_i - P_{i+1}|) / (P_i)$ exceeds γ for baseline method 1 and Pattern_Order. We characterize this difference as $\delta T_{thB1} = (T_{thBaseline1} - T_{thPattern_Order}) / (T_{thBaseline1}) \times 100\%$; $T_{thBaseline1}$ and $T_{thPattern_Order}$ are the measures (defined in Section IV) obtained using the first baseline method and the Pattern_Order heuristic, respectively. The value of γ is chosen to be 0.05 (i.e., 5%) to highlight the flatness in power profiles obtained using the different techniques.
- 5) The indicators δT_{thB2} and δT_{thB3} are determined in a similar fashion as δT_{thB1} .
- 6) For the ISCAS'89 and IWLS'05 benchmark circuits, the aforementioned results are reported for both the ILP method and the Pattern_Order heuristic.
- 7) For selected benchmark circuits, the aforementioned results are reported for the ILP-based heuristic technique.

TABLE III
PERCENTAGE REDUCTION IN THE VARIANCE OF TEST POWER CONSUMPTION OBTAINED
USING THE Pattern_Order HEURISTIC FOR SELECTED IWLS'05 BENCHMARK CIRCUITS

Circuit	N	No. of flip-flops	No. of cells	No. of scan chains	P_{max}	Baseline 1		Baseline 2		Baseline 3	
						δV_{B1}	$\delta T_{th_{B1}}$	δV_{B2}	$\delta T_{th_{B2}}$	δV_{B3}	$\delta T_{th_{B3}}$
systemcaes	294	1008	17817	1	570	9.55	8.93	7.31	7.08	9.94	9.62
					580	6.67	6.48	4.70	4.58	7.29	7.66
					590	6.53	2.81	4.64	1.90	7.19	7.61
usb_funct	237	1918	25510	1	1030	7.14	6.83	5.91	5.77	7.62	7.48
					1040	4.52	4.04	2.23	1.91	5.05	4.96
					1060	4.27	3.95	1.69	1.34	4.87	4.54
ac97_ctrl	230	2302	28049	1	1055	12.32	11.98	10.61	10.49	12.73	12.24
					1065	12.18	11.43	9.87	9.14	12.45	12.09
					1075	11.66	10.93	9.21	8.87	12.14	11.58
wb_conmax	413	3316	59483	1	1520	5.12	5.08	4.37	4.11	5.91	5.75
					1530	4.63	4.42	4.04	3.98	4.80	4.66
des_perf	346	9105	146224	1	5660	8.39	7.87	6.71	6.63	8.58	8.33
					5670	8.12	7.94	6.27	6.01	7.93	7.67
					5680	7.48	7.20	5.51	5.63	7.62	7.56

TABLE IV
PERCENTAGE REDUCTION IN THE VARIANCE OF TEST POWER CONSUMPTION OBTAINED USING THE ILP-BASED HEURISTIC

Circuit	N	n	No. of scan chains	P_{max}	Baseline 1		Baseline 2		Baseline 3	
					δV_{B1}	$\delta T_{th_{B1}}$	δV_{B2}	$\delta T_{th_{B2}}$	δV_{B3}	$\delta T_{th_{B3}}$
s9234	231	290	1	155	13.94	14.06	8.19	11.76	15.61	17.12
				165	10.39	14.66	7.82	9.24	8.68	9.62
				175	9.54	18.83	6.68	7.57	5.42	5.91
			4	155	14.53	12.14	9.28	10.12	7.43	8.15
				165	8.12	12.41	8.92	9.48	7.74	9.02
				175	4.83	8.24	4.19	4.54	3.67	3.98
			8	155	11.44	14.16	4.43	3.08	8.41	8.93
				165	4.21	8.86	0.63	0.72	3.67	4.06
				175	3.75	7.21	0.92	1.36	4.88	5.61
s13207	311	723	1	460	5.39	6.41	1.46	4.84	5.26	5.97
				470	2.74	3.18	0.93	1.76	2.98	3.05
				480	2.73	3.16	0.92	1.76	2.97	3.03
			4	460	2.90	3.43	0.50	2.52	3.17	3.83
				470	3.18	3.66	0.84	0.92	3.72	4.04
				480	3.14	3.53	0.80	0.89	3.41	3.63
			8	460	2.90	3.43	0.50	2.52	3.17	3.83
				470	3.18	3.66	0.84	0.92	3.72	4.04
				480	3.14	3.53	0.80	0.89	3.41	3.63
systemcaes	294	1008	1	570	7.82	7.43	5.92	5.84	8.39	8.11
				580	6.33	6.21	4.52	4.17	7.04	6.90
				590	5.86	5.94	4.91	5.14	6.28	6.63
			4	570	5.13	5.67	4.36	4.14	5.29	5.94
				580	4.89	5.21	4.17	4.01	4.96	5.11
				590	4.59	4.33	3.62	3.74	4.71	4.48
			8	580	2.74	3.19	1.87	2.28	3.07	2.92
				590	2.41	2.68	1.53	1.48	2.90	2.79
				590	2.41	2.68	1.53	1.48	2.90	2.79
wb_conmax	294	1008	1	1520	5.19	5.33	3.47	3.21	5.95	5.68
				1530	4.72	4.80	3.03	3.16	4.69	6.21
			4	1520	4.56	4.08	2.95	3.27	4.12	3.65
				1530	3.61	3.89	2.33	2.48	2.90	2.74

8) The reduction in the variance of test power are reported for the ISCAS'89 and IWLS'05 benchmark circuits with a single scan chain, using t -detect test sets.

We use a commercial ATPG tool to generate t -detect ($t = 1, 3, 5$) stuck-at patterns (and responses) for the ISCAS'89 and IWLS'05 benchmarks. The experimental results for four ISCAS'89 and IWLS'05 benchmark circuits obtained using ILP and the Pattern_Order heuristic are shown in Table I. The reduction on power variation using ILP, as expected, is greater than that obtained using the heuristic method; however, the Pattern_Order heuristic is also efficient for reordering the test patterns for WLTBI. Fig. 6 illustrates the impact of TC_{th} on the percentage savings in test power variation. It is observed that higher (relaxed) values of TC_{th} result in reduced savings

in test power variation for s5378; similar results are observed for other circuits.

The results for five larger ISCAS'89 benchmark circuits are listed in Table II. The experimental results for the five IWLS'05 benchmark circuits are listed in Table III. A description of the IWLS'05 benchmarks in terms of the number of scan flip-flops and total number of cells is shown in Table III. The values of P_{max} (measured in terms of the number of flip-flop transitions) for each circuit are chosen carefully after analyzing the per-cycle test power data. We also present experimental results obtained using the ILP-based heuristic technique for five benchmark circuits in Table IV. The Pattern_Order heuristic results in better savings in power variation compared with the ILP-based heuristic; the ILP-based heuristic however is a good

TABLE V
PERCENTAGE REDUCTION IN THE VARIANCE OF TEST POWER CONSUMPTION OBTAINED USING THE Pattern_Order HEURISTIC FOR SELECTED BENCHMARK CIRCUITS USING t -DETECT TEST PATTERNS

Circuit	n	N	t -detect	P_{max}	Baseline 1		Baseline 2		Baseline 3	
					δV_{B1}	δT_{thB1}	δV_{B2}	δT_{thB2}	δV_{B3}	δT_{thB3}
s5378	313	363	$t = 3$	150	8.19	7.63	5.48	5.06	9.26	9.45
				155	6.92	7.14	4.03	3.70	7.57	7.72
		586	$t = 5$	150	7.31	7.65	4.98	5.13	8.10	8.22
				155	7.16	7.49	4.41	4.64	7.73	7.62
s9234	290	349	$t = 3$	150	17.12	19.46	7.03	9.64	13.39	15.94
				160	7.40	9.14	4.32	7.26	9.13	10.29
				170	4.95	5.43	3.89	3.96	7.14	8.41
		539	$t = 5$	150	13.81	15.02	10.48	11.37	16.17	17.26
				160	7.08	7.93	6.42	7.21	9.15	9.87
				170	4.11	5.03	3.74	4.36	5.69	6.56
s38417	764	436	$t = 3$	390	5.14	5.89	3.96	4.08	5.42	5.63
				405	4.78	4.92	3.12	3.33	5.31	5.74
				415	2.01	2.26	0.79	1.07	2.45	2.63
		679	$t = 5$	390	6.38	6.72	5.15	5.41	6.93	6.86
				405	5.85	6.11	4.32	4.47	6.74	6.88
				415	3.53	3.38	2.06	2.23	3.87	4.10
ac97_ctrl		394	$t = 3$	1065	7.39	7.68	4.92	5.04	7.22	7.43
				1075	7.08	6.84	4.29	4.16	6.67	7.09
		512	$t = 5$	1065	9.14	8.63	6.19	6.27	9.89	9.51
				1075	8.76	8.83	5.47	5.29	9.14	9.37
wb_conmax		718	$t = 3$	1520	12.94	13.18	9.13	9.27	12.87	12.52
				1530	12.22	12.40	8.58	8.61	11.95	11.86
		897	$t = 5$	1520	13.72	14.19	11.87	11.45	14.13	14.62
				1530	13.04	13.85	10.74	10.67	13.59	13.91

alternate solution method for ordering test patterns. We use the smallest value of TC_{th} necessary to construct a valid ordering for the results in Table IV. Experimental results obtained using t -detect test sets for five benchmark circuits are presented in Table V.

The ordering of test patterns using the ILP-based technique yields lower variation in test power compared to the heuristic method. The Pattern_Order heuristic is, however, an efficient method for circuits with a large number of test patterns. The results show that a significant reduction in test power variation can be obtained using the proposed ordering technique. The test-pattern ordering technique also results in low cycle-to-cycle variation in test power consumption. The ILP-based heuristic technique can also be used as an effective technique to determine the ordering of test patterns for WLTBI. This reduction in test power variation obtained using the ILP-based heuristic technique is comparable to the Pattern_Order heuristic.

Even small reductions in the variations in test power can contribute significantly toward reducing yield loss and test escape during WLTBI. We know from (1) that the junction temperature of the device varies directly with the power consumption. This indicates that a 10% variation in device power consumption will lead to a 10% variation in junction temperatures; this can potentially result in thermal runaway (yield loss), or under burn-in (test escape) of the device. The importance of controlling the junction temperature for the device to minimize post-burn-in yield loss is highlighted in [25].

All experiments were performed on a 2.4-GHz AMD Opteron processor, with 4 GB of memory. The CPU times for optimal ordering of test patterns using ILP ranges from 16 min for s1423 to 6 h for s5378. The CPU times for ordering test patterns using the Pattern_Order heuristic, when the cycle-accurate power information is given, is in the order of minutes (the maximum being

120 min for s13207). The CPU time to construct the cycle-accurate power information is in the order of hours for the benchmark circuits.

VIII. CONCLUSION

We have formulated a test-pattern ordering problem to minimize power variations during WLTBI. The pattern-ordering approach is based on cycle-accurate power information for the device under test. An exact solution technique has been developed based on ILP. Heuristic techniques have also been presented to solve the pattern-ordering problem. We have compared the proposed reordering techniques to baseline methods that minimize peak power and average power, as well as a random-ordering method. In addition to computing the statistical variance of the test power, we have also quantified the flatness of the power profile during test application. Experimental results for the ISCAS'89 and the IWLS'05 benchmark circuits show that there is a moderate reduction in power variation if patterns are carefully ordered using the proposed techniques. Since the junction temperatures in the device under test are directly proportional to the power consumption, even small reductions in the power variance offer significant benefits for WLTBI.

REFERENCES

- [1] International Technology Roadmap for Semiconductors, "Assembly and packaging," 2005. [Online]. Available: <http://www.itrs.net/Links/2005ITRS/AP2005.pdf>
- [2] L. Yan and J. R. English, "Economic cost modeling of environmental-stress-screening and burn-in," *IEEE Trans. Reliab.*, vol. 46, no. 2, pp. 275–282, Jun. 1997.
- [3] P. C. Maxwell, "Wafer-package test mix for optimal defect detection and test time savings," *IEEE Des. Test. Comput.*, vol. 20, no. 5, pp. 84–89, Sep./Oct. 2003.

- [4] Delta V Instruments, Richardson, TX, "A comparison of wafer level burn-in & test platforms for device qualification and known good die (KGD) production," [Online]. Available: http://www.delta-v.com/images/White_Paper_-_Comparing_WLBT_Platforms.pdf
- [5] M. F. Zakaria, Z. A. Kassim, M. P. Ooi, and S. Demidenko, "Reducing burn-in time through high-voltage stress test and Weibull statistical analysis," *IEEE Des. Test. Comput.*, vol. 23, no. 2, pp. 88–98, Mar./Apr. 2006.
- [6] T. J. Powell, J. Pair, M. John, and D. Counce, "Delta IDDQ for testing reliability," in *Proc. VLSI Test Symp.*, 2000, pp. 439–447.
- [7] P. Tadayon, "Thermal challenges during microprocessor testing," *Intel Technol. J.*, vol. 3, pp. 1–8, 2000.
- [8] "IWLS 2005 Benchmarks," 2005. [Online]. Available: <http://iwls.org/iwls2005/benchmarks.html>
- [9] I. Y. Khandros and D. V. Pedersen, "Wafer-level burn-in and test. U. S. Patent Office," U.S. Patent 6 064 213, May 16, 2000.
- [10] A. Singh, P. Nigh, and C. M. Krishna, "Screening for known good die (KGD) based on defect clustering: An experimental study," in *Proc. Int. Test Conf.*, 1997, pp. 362–371.
- [11] T. Mckenzie, W. Ballouli, and J. Stroupe, "Motorola wafer level burn-in and test," in *Proc. Burn-in Test Socket Workshop*, 2001 [Online]. Available: http://www.swtest.org/swtw-library/2002proc/PDF/T02_Mckenzie.pdf
- [12] P. Pochmuller, "Configuration for carrying out burn-in processing operations of semiconductor devices at wafer level. U. S. Patent Office," U.S. Patent 6 535 009, Mar. 18, 2003.
- [13] P. Nigh, "Scan-based testing: The only practical solution for testing ASIC/consumer products," in *Proc. Int. Test Conf.*, 2002, p. 1198.
- [14] J. Forster and C. Lopez, "Junction temperature during burn-in: How variable is it and how can we control it?," in *Proc. Semicond. Thermal Meas. Manage. Symp.*, 2007, pp. 168–173.
- [15] A. Benso, A. Bosio, S. D. Carlo, G. D. Natale, and P. Prinetto, "ATPG for dynamic burn-in test in full-scan circuits," in *Proc. Asian Test Symp.*, 2006, pp. 75–82.
- [16] Y. Zorian, "A distributed BIST control scheme for complex VLSI devices," in *Proc. VLSI Test Symp.*, 1993, pp. 4–9.
- [17] S. Wang and S. K. Gupta, "An automatic test pattern generator for minimizing switching activity during scan testing activity," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 21, no. 8, pp. 954–968, Aug. 2002.
- [18] P. Girard, "Survey of low-power testing of VLSI circuits," *IEEE Des. Test. Comput.*, vol. 19, no. 3, pp. 80–90, May/Jun. 2002.
- [19] R. Sankaralingam, R. R. Oruganti, and N. A. Toubia, "Static compaction techniques to control scan vector power dissipation," in *Proc. VLSI Test Symp.*, 2000, pp. 35–40.
- [20] K. M. Butler, J. Saxena, A. Jain, T. Fryars, J. Lewis, and G. Hetherington, "Minimizing power consumption in scan testing: Pattern generation and DFT techniques," in *Proc. Int. Test Conf.*, 2004, pp. 355–364.
- [21] J. Saxena, K. M. Butler, and L. Whetsel, "An analysis of power reduction techniques in scan testing," in *Proc. Int. Test Conf.*, 2001, pp. 670–677.
- [22] X. Wen, Y. Yamashita, S. Kajihara, L. T. Wang, K. K. Saluja, and K. Kinoshita, "On low-capture-power test generation for scan testing," in *Proc. VLSI Test Symp.*, 2005, pp. 265–270.
- [23] V. Dabholkar, S. Chakravarty, I. Pomeranz, and S. M. Reddy, "Techniques for minimizing power dissipation in scan and combinational circuits during test application," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 17, no. 12, pp. 1325–1333, Dec. 1998.
- [24] P. K. Latypov, "Energy saving testing of circuits," *Autom. Remote Control*, vol. 62, pp. 653–655, Apr. 2001.
- [25] A. Vassighi, O. Semenov, and M. Sachdev, "Thermal runaway avoidance during burn-in," in *Proc. Int. Rel. Phys. Symp.*, 2004, pp. 655–656.
- [26] K. Kanda, K. Nose, H. Kawaguchi, and T. Sakurai, "Design impact of positive temperature dependence on drain current in sub-IV CMOS VLSIs," *IEEE J. Solid-State Circuits*, vol. 36, no. 10, pp. 1559–1564, Oct. 2001.
- [27] S. Bahukudumbi and K. Chakrabarty, "Power management for wafer-level test during burn-in," in *Proc. Asian Test Symp.*, pp. 231–236.
- [28] M. E. Imhof, C. G. Zoellin, H. Wunderlich, N. Maeding, and J. Leenstra, "Scan test planning for power reduction," in *Proc. Des. Autom. Conf.*, 2007, pp. 521–526.
- [29] P. M. Rosinger, B. M. Al-Hashimi, and N. Nicolici, "Power profile manipulation: A new approach for reducing test application time under power constraints," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 21, no. 10, pp. 1217–1225, Oct. 2002.
- [30] J. Costa, P. F. Flores, H. C. Neto, J. C. Monteiro, and J. P. Marques-Silva, "Exploiting don't cares in test patterns to reduce power during BIST," in *Proc. Eur. Test Workshop*, 1998, pp. 34–36.
- [31] P. Girard, C. Landrault, S. Pravossoudovitch, and D. Severac, "Reducing power consumption during test application by test vector ordering," in *Proc. IEEE Int. Symp. Circuits Syst.*, 1998, pp. 24–27.
- [32] P. Girard, L. Guiller, C. Landrault, and S. Pravossoudovitch, "A test vector ordering technique for switching activity reduction during test operation," in *Proc. IEEE Great Lake Symp. VLSI*, 1999, pp. 24–27.
- [33] S. Ghosh, S. Basu, and N. A. Toubia, "Joint minimization of power and area in scan testing by scan cell reordering," in *Proc. Annu. Symp. VLSI*, 2003, pp. 246–249.
- [34] Y. Bonhomme, P. Girard, L. Guiller, C. Landrault, and S. Pravossoudovitch, "Efficient scan chain design for power minimization during scan testing under routing constraint," in *Proc. Int. Test Conf.*, 2003, pp. 488–493.
- [35] Z. Zhang, S. M. Reddy, I. Pomeranz, J. Rajski, and B. M. Al-Hashimi, "Enhancing delay fault coverage through low power segmented scan," in *Proc. Eur. Test Symp.*, 2006, pp. 21–28.
- [36] S. Samii, E. Larsson, K. Chakrabarty, and Z. Peng, "Cycle-accurate test power modeling and its application to SOC test scheduling," in *Proc. Int. Test Conf.*, 2006, pp. 1–10.
- [37] G. L. Vairaktarakis, "On Gilmore–Gomory's open question for the bottleneck TSP," *Comput. Oper. Res.*, vol. 31, pp. 483–491, Nov. 2003.
- [38] M. Garey and D. Johnson, *Computers and Intractability: A Guide to the Theory of NP-Completeness*. San Francisco, CA: Freeman, 1979.
- [39] R. Y. Rubinfeld and D. P. Kroese, *A Unified Approach to Combinatorial Optimization, Monte-Carlo Simulation, and Machine Learning*. New York: Springer-Verlag, 2004.

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