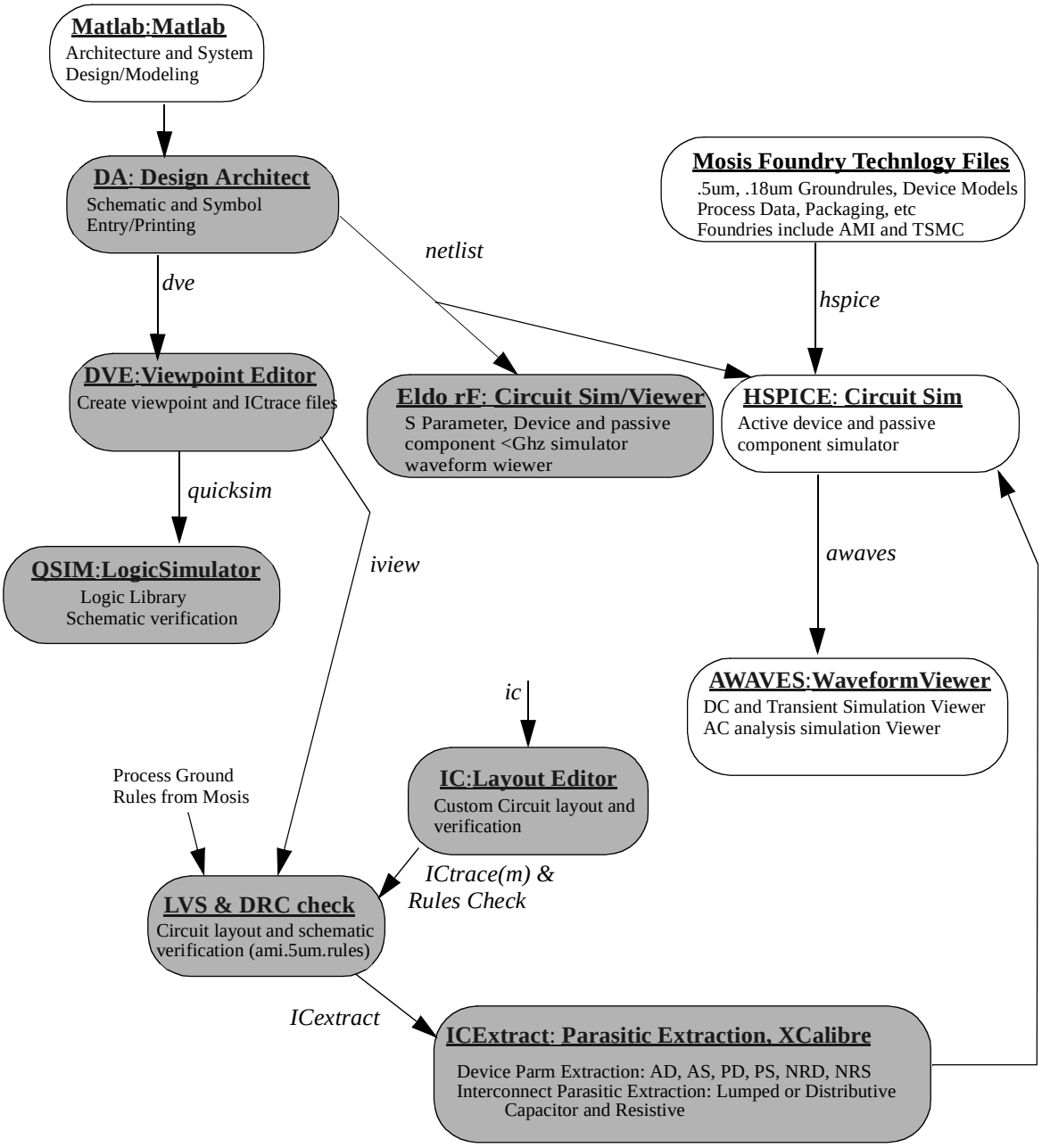
FIGURE 1. **Mixed-Signal CAD Software Data Flow**



Shaded software tools are provided by Mentor Graphics Corporation

The Hspice and Awaves tools are provided by Synopsis.

The Matlab and Matlab toolboxes are provided by Mathworks.

SOFTWARE NOTES:

Design Architect (DA): This Mentor tool is a schematic based circuit editor that allows the user to draw desired components and circuit schematics quite effectively. To initiate the program type ‘da’ at the unix prompt. There are two important levels within each circuit schematic. The first level is designated as the ‘sheet.’ At this level, the basic circuit drawings are made. This schematic can then be represented as ‘symbol’ in the next level of hierarchy. To link the ‘sheet’ to the ‘symbol,’ the input/output port names must match, and both levels must be saved under the same name (and pathname). It is recommended that each user set up a Soft Name reference pathname file to point to desired directories. One such pathname should be $AMILIBNETS. This particular pathname points to a directory where a library of basic components have been set up for your use. Editing and placing objects within a sheet and symbol can be done with the right side panel, the pull-down menu along the top, and the function keys specified along the bottom of the screen. Creating and editing these schematics will go much faster if the identical commands were specified by the with the middle mouse button or by simply typing in the command. When the middle mouse button is held down, a red line pattern can be draw to initiate a command. To see the menu of stroke commands draw a ‘?’ with the middle mouse button. When a character is typed by the user a dialogue box opens showing the characters typed to call a specified command. One last shortcut to take advantage of is the drag and copy procedure. Since the program can support many window of different schematics or symbols, it is very easy to copy part or all of the schematic from one window to another. This can be very useful if the drawing are similar and only minor alteration are needed instead of the redoing the entire drawing. One note of warning with this copy procedure, however, make sure not to copy between sheet and symbols drawings because these editing protocols are completely different. Remember the levels of hierarchy between sheet and symbol. To add a symbol into a schematic, the add symbol command must be used. When you are finished with your drawing make sure to check your work for errors under the check ‘sheet’ or ‘symbol’ pull down menu. You may get both ‘errors9’ and ‘warnings’ when a check report is compiled, it is important to fix the cause of the ‘errors’ before the ‘warnings’ because they mean that your drawing has failed the check. The final step is to save your work. To produce printouts DA must be set up on a Washington terminal, and the printer setup must be changed to say ‘hpdsil at dsil lab printer.’ The selected drawing may then be printed out to the printer in Rm 161by choosing the print command under the File menu.

IC Station: This tool is a layout editor for chip design and can be started by typing 'ic' on the unix prompt. The editor produces the actual dimensions and contours within the chip of your particular circuit. To look at some familiar layouts point to $AMILIBLAY for some of the basic elements needed for layout procedures. If the layout already exist you can hit the 'Open' command button on the right panel and navigate to the desired location of the layout. The create a new layout, hit the 'create' button to open a dialogue box. Under name type the pathname of the desired layout and under process point to the following directory and file $TECHFILES/scmos. Once a layout window is open, it would be helpful to setup some hotkeys on your keyboard to go along with the function keys, edit menus, and the edit panel along the right panel. To enable hotkeys go under the 'Other' menu to 'hotkeys' and then to 'enable.' Load in a file called 'keypad' from the $TECHFILES directory. The keypad operations can be seen in Appendix A(?) of this manual. Your now have the basic tools setup to setup. As in DA, this tool also takes advantage of a hierarchical system with each individual layout cell. A cell that is added into a higher level cell can be replicated, positions, and oriented within the main cell. The program also allows the user to drive into a lower level cell for editing by setting the 'contest.' The next few descriptions will describe the checking procedure employed under the ICstation program.

ICrules(DRC):Design Rules Check can be enabled be clicking on the ICrules push button on the main right panel window. This should open the ICrules panel of options. First load the desired rules file by hitting the 'load rules' button. With the dialogue box now open navigate down to $TECHFILES/ami.5um.rules and then hit OK. You can start checking your layout by clicking the 'check' button and specifying the area to be check with the cursor (or just enter to check the entire cell). The program will check for minimum spacing errors based on specified rules file (See Appendix B for a complete listing). Once the check is complete, the total number of error will be displayed along the bottom comment box. If you have zero errors, your cell has passed the check. But if you have any error you can view then individually by clicking on 'first' then 'next.' The ideal with this rules check is the pack the cell in as tight as possible without breaking any rules.

ICtrace(LVS): The LVS check will verify your layout to the corresponding schematic drawing from DA. To provide that link between the IC and DA, a viewpoint files must be created under the DA schematics. A viewpoint is created under the a program called Design Viewpoint Editor(DVE). Before LVS checking, however, ports of the same name as the schematics must be made in the layout. Select the layer to be make into a port and go under the 'Connection' menu/make port, then specify the type of signal and name of the port. For the actual checking procedure, first hit the ICtrace(M) button on the main right pane and then hit the 'LVS' button to open another dialogue box. Under the source box point to the pathname of the veiwpoint you just created. Then hit the 'Setup LVS prop' button to set the appropriate tolerance levels of your check. Hitting OK will initiate the checking procedure. Once the check is completed, you may look at the report under 'LVS/report.' If the connections and properties from your schematic match your layout you should get a happy face to show you are indeed correct. If you are incorrect you should get a X in the report and have to do some more debugging.

Design Viewpoint Editor(DVE):A viewpoint is a dataset which correlates a the schematic graphical database to a layout graphical database. To initiate the program type ‘dve’ at the prompt. Once the program is open, hit the ‘Add VPT’ button on the right panel to open a dialogue box, then point to the desired schematic name and type in the viewpoint name in the appropriate box. A couple of window should open to allow you to create the specific properties. Next hit the ‘Add PT’ button to open a Add Primitive dialogue box. In the box, type ‘element’ for the name and ‘mn,’ ‘mp,’ ‘c,’ and ‘r’ under the property boxes. Save the viewpoint and your ready to go back into ICstation to do a LVS check.

Netlist & Hspice: This particular tool allows the user the check the viability of a potential circuit before a layout is processed. Hspice is of course a circuit simulator that involves special codes for names and properties, which can become somewhat tedious for large circuits. Therefore a ‘netlist’ command can be used to extract the needed information from the DA schematics themselves. To execute the command just type ‘netlist pathname.’ A file called ‘spice_out,’ which contains the spice codes of the circuit, should then be stored in your directory. You can change the name of the file, make the appropriate input voltage commands, operation commands, and then initiate the spice simulation to check your circuit. To run hspice you must be remotely login to Jefferson. Just type ‘hspice’ on the prompt and it should ask you for the file name. Once the simulation is complete several output files are generated. The main output file is contained in the *.lis. A special graphical file is created in the *.tr0 file. This file is utilized in the Awaves program.

Awaves: This program is a simple graphical tool that allows you to view input/output waveforms from hspice circuit simulation. To execute mwaves type ‘mwaves *.tro’ which should open the program window. A Result Browser window should also open which enables the user to choose the particular waveforms to view. The x-axis is usually specified as time and frequency, while the y-axis can be seen by double clicking the waveform name with right mouse button. Multiple panels may be added to view another set of waveforms on a different x-y axis, and zoom in/out operations are easily performed.

ICextract: The extract program is two fold. Firstly, this program will generate a spice netlist which includes spice parameters L, W, AS, AD, PS, PD, NRD, NRS. These parameters are calculated based on the ami.5um.rules file and device layout dimensions. The spice schematic will include the pmos and nmos devices which correlate to the viewpoint which references the schematic. Secondly, the program will extract either distributed or lumped parasitics (resistive and capacitor) of metal 1 through metal 3 and create a spice netlist of these parameters for spice simulation. For this parasitic extraction, the output spice netlist can be very large which is based on the complexity and size of the layout. X-Calibre is another extract provided by Mentor Graphics and is currently being setup for .18um process technology.

Matlab: This tool will be used for high level modeling and analysis for circuit systems. It can also be used to validate spice simulation. The Matlab toolboxes provide a variety of linear system analysis tools that are used for analog system level design modeling.

Eldo RF simulator: This tool is used for high frequency RF and microwave simulations which are simulations above 1 Ghz that require S-parameter spice models. Harmonic balancing simulations, transient simulations and ac analysis can be performed at circuit and system level.