

Combination Lock

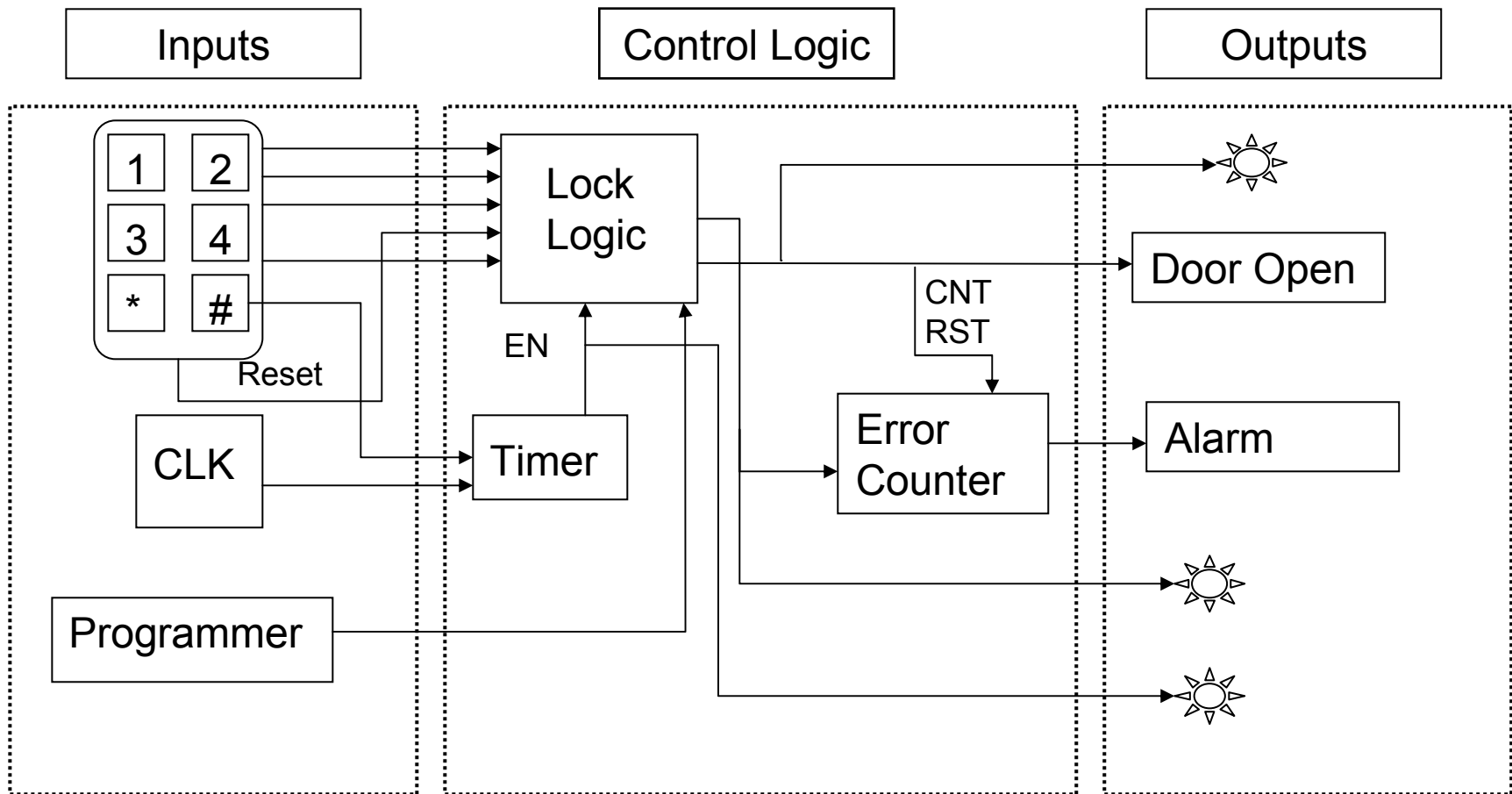
ECE261: VLSI
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Features

- Multiple users with different password protection for each user.
- User friendly indicators using LEDs.
- Time out for incorrect entries.
- External programmability.
- External display to show invalid/valid entry

Block diagram

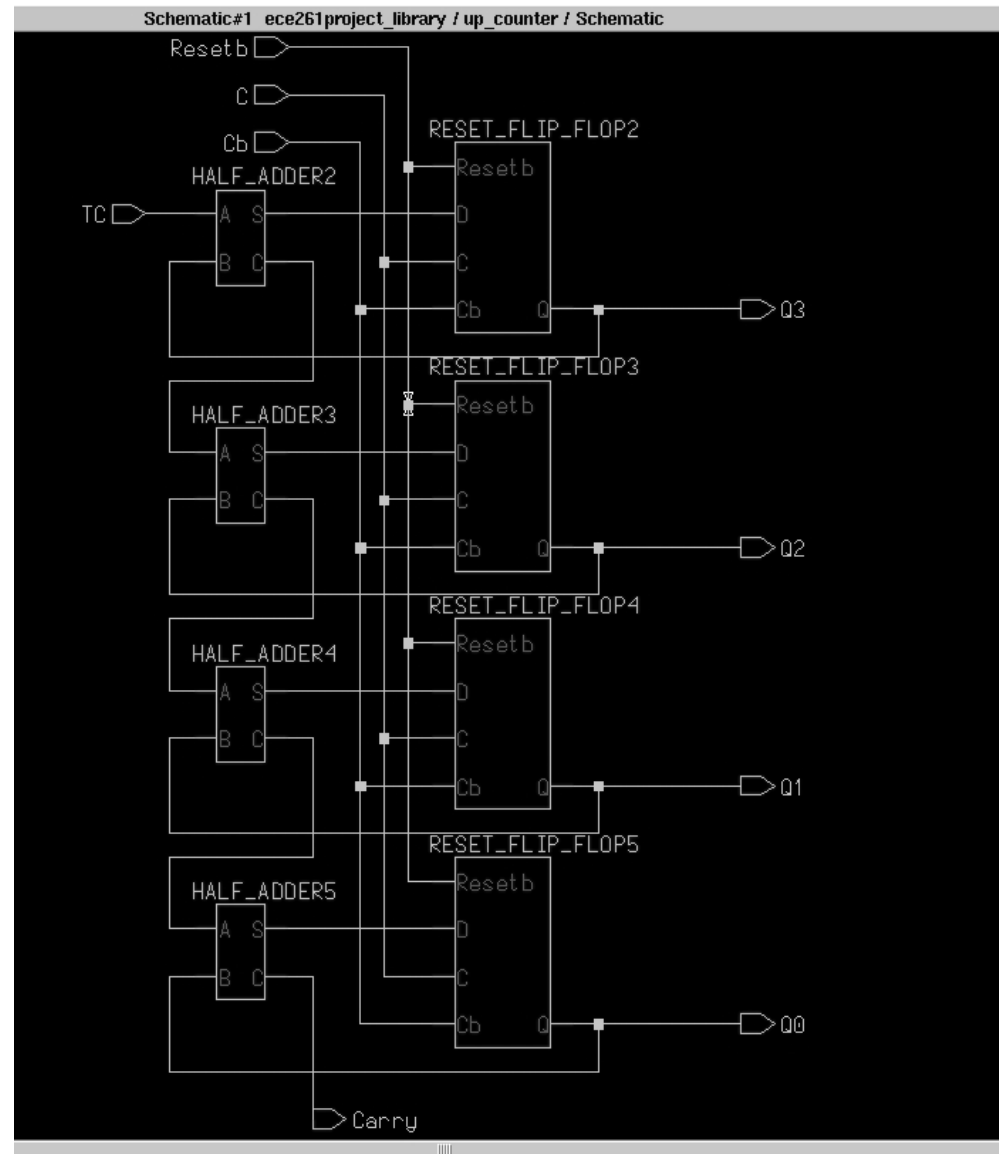


Active Timer

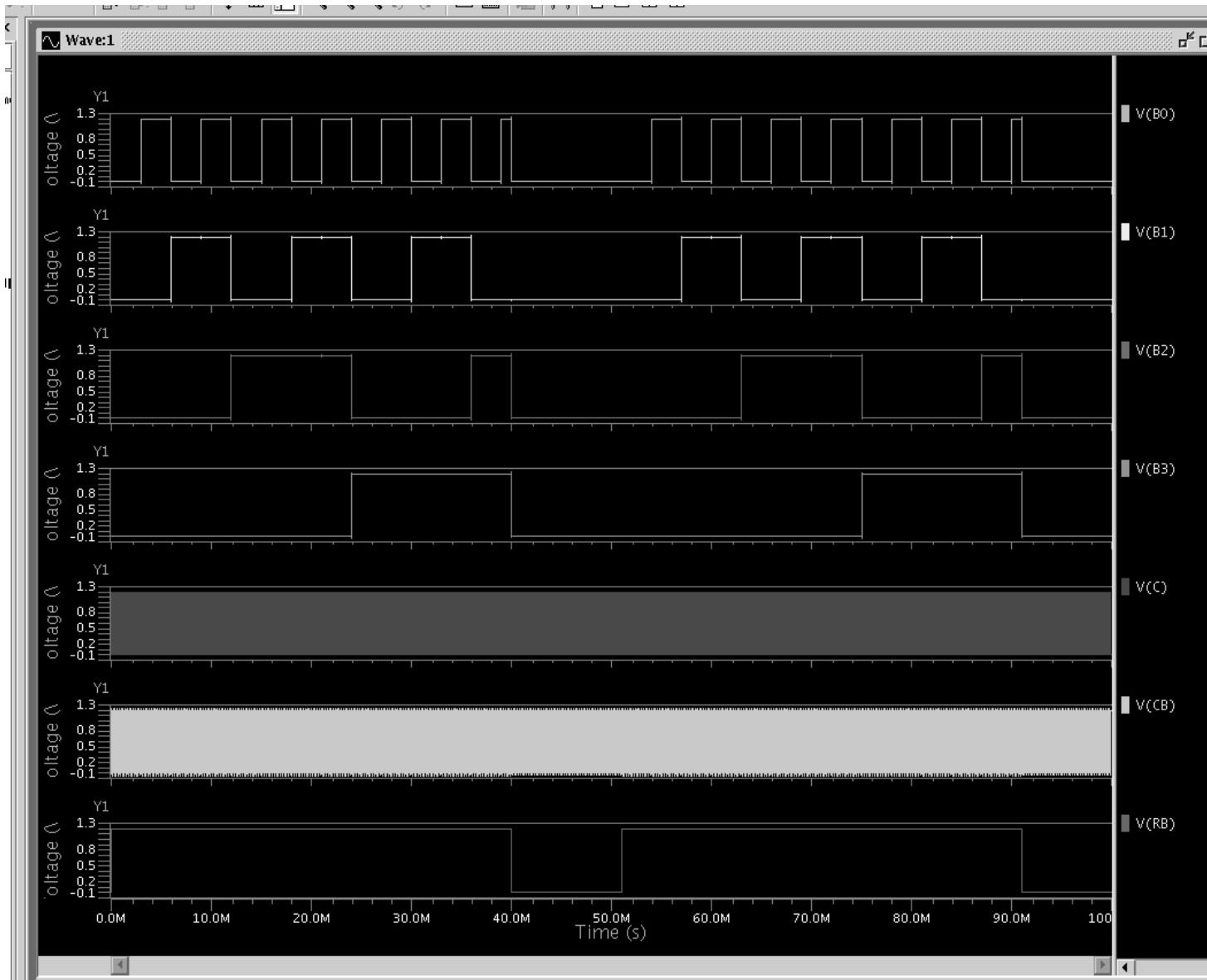
- Timer reads from a 5KHz clock signal and remains active for 10sec.
- Sets the enable for reading inputs from external keypad.
- Utilizes cascaded D flip flop counter circuit.
- Asynchronous counter reset.

Active Timer

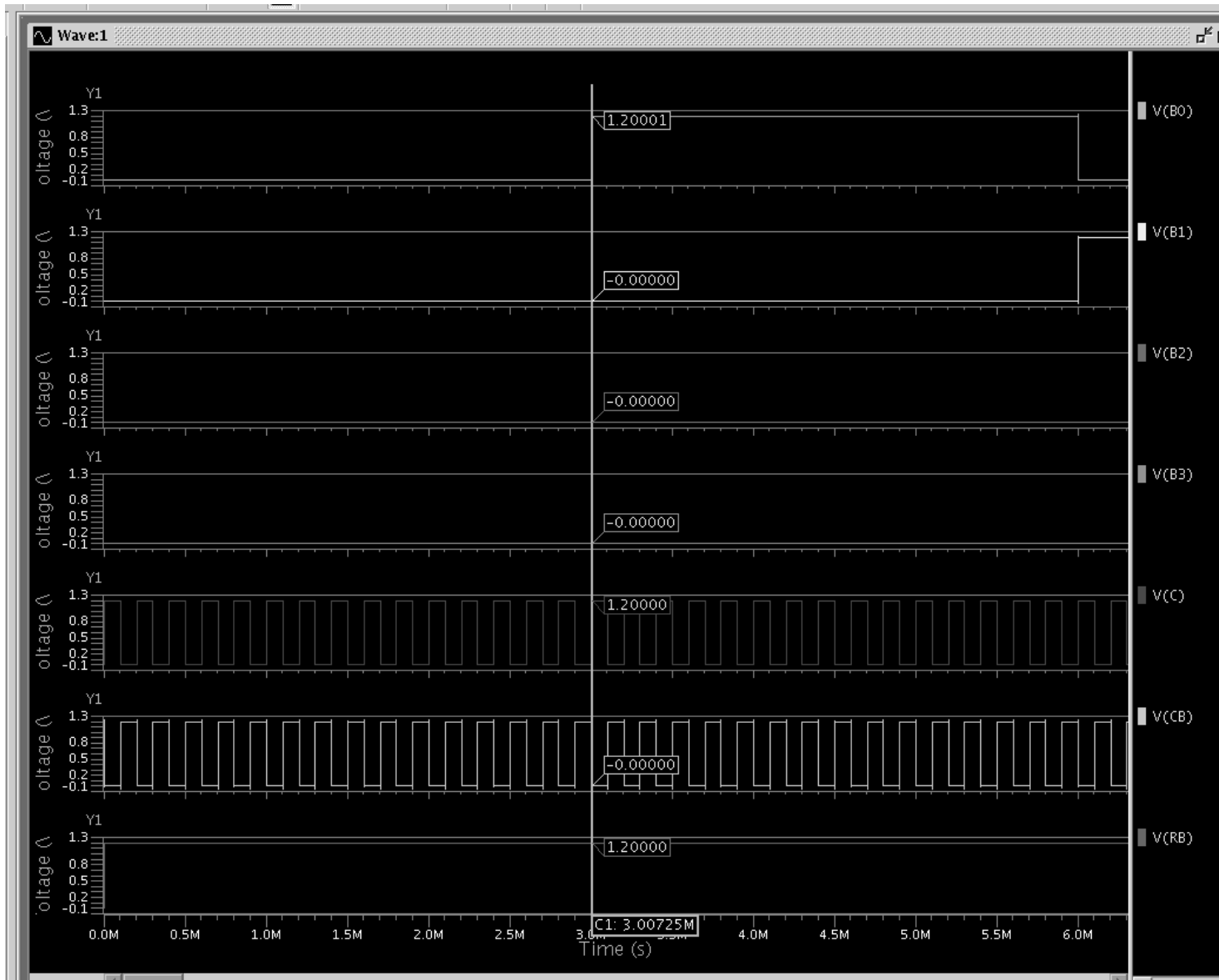
➤ Up counter



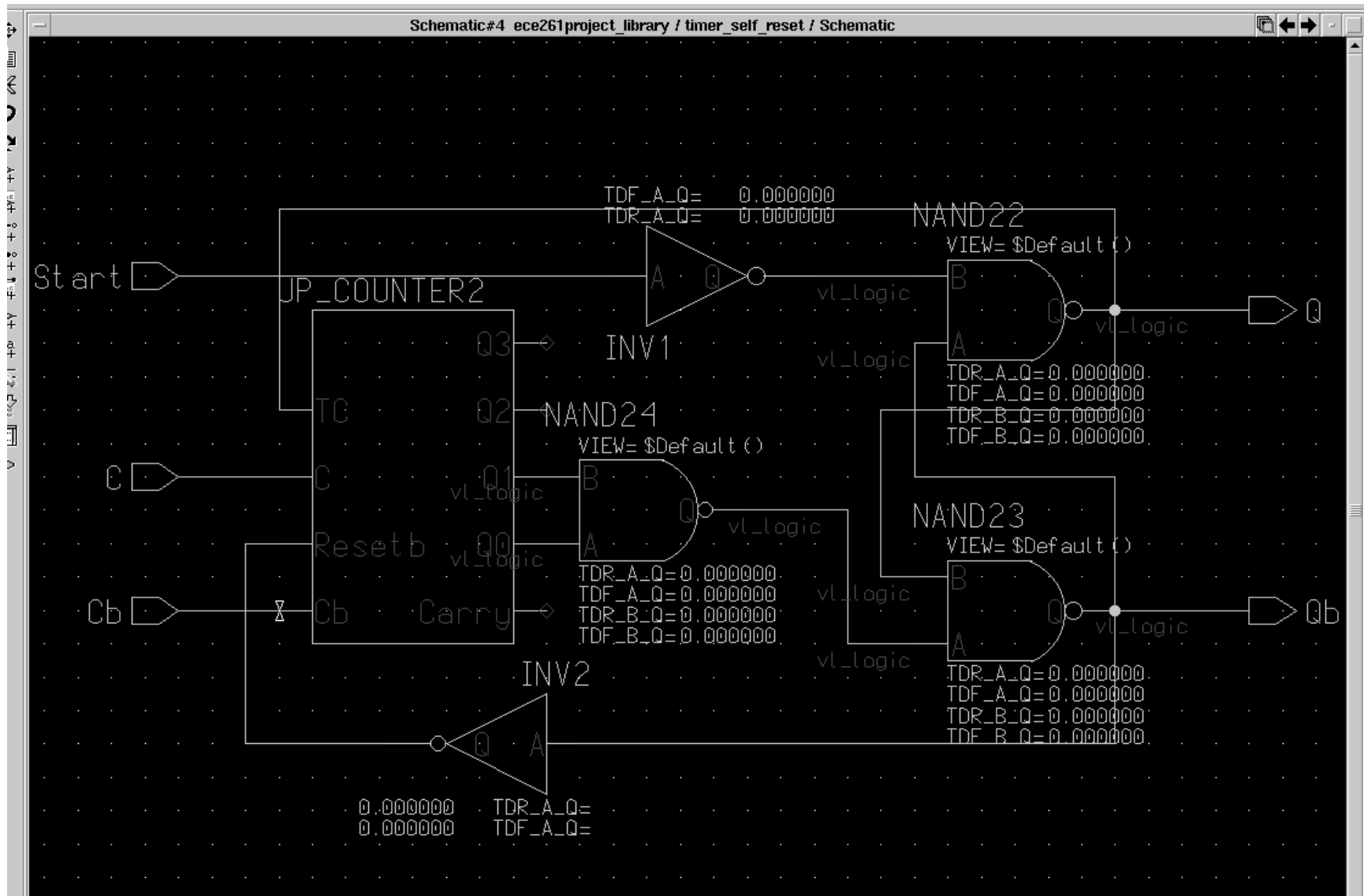
Active Timer Sim



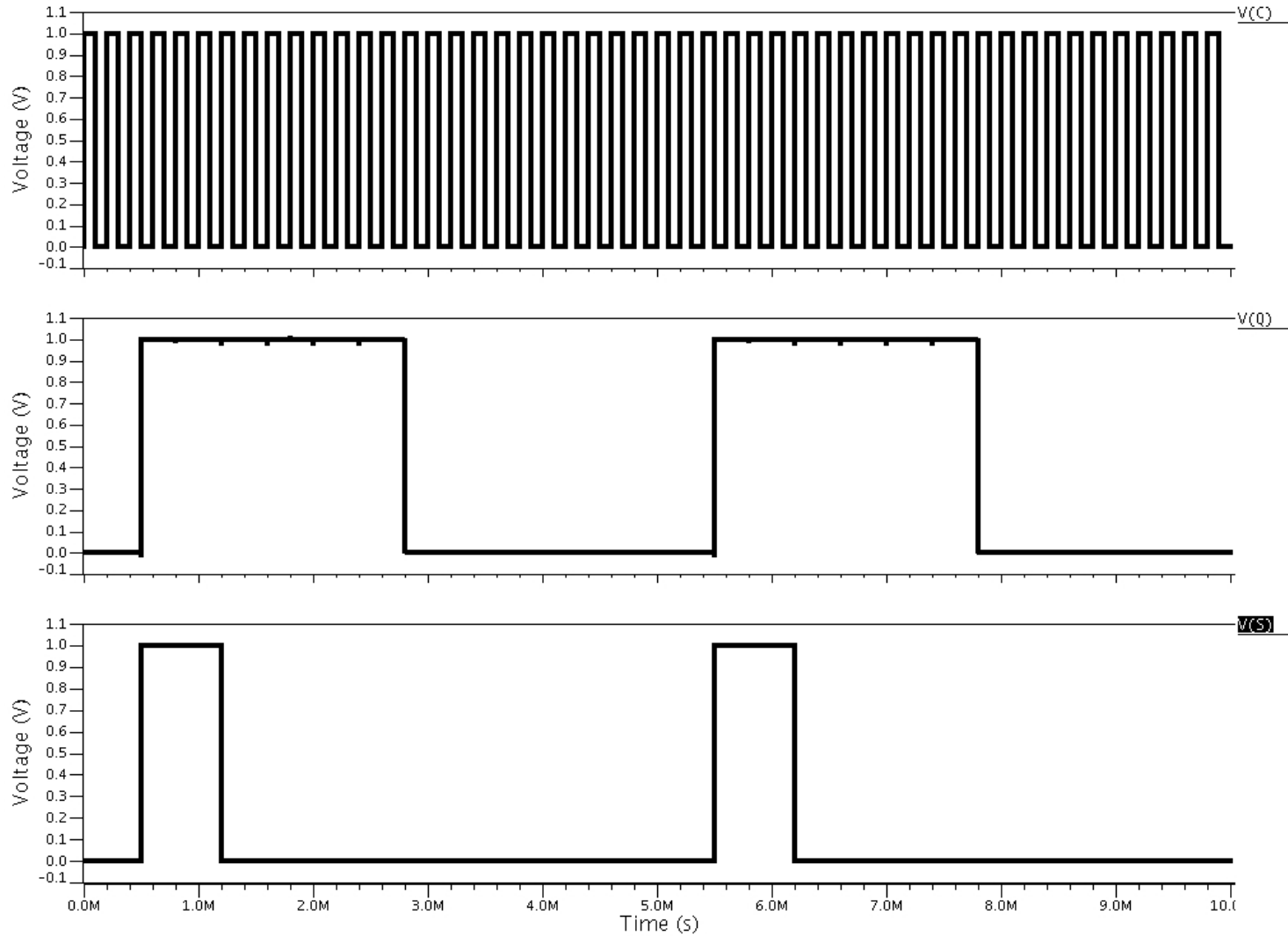
Active Timer Sim



Active Timer Control

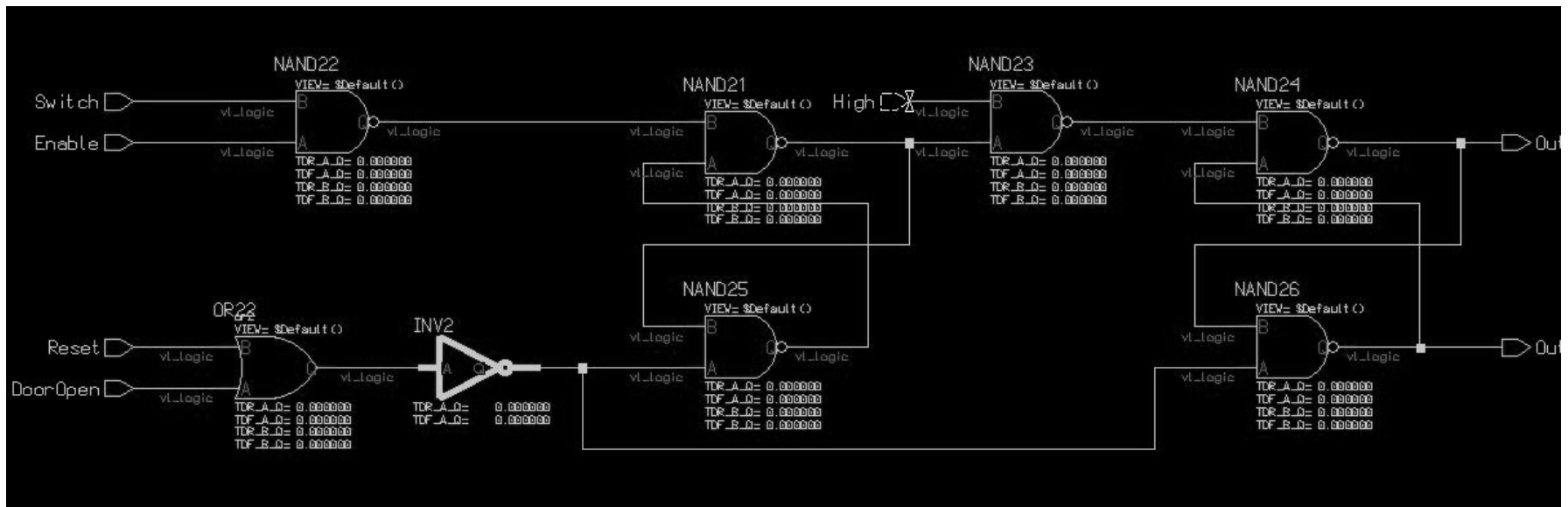


Active Timer Control

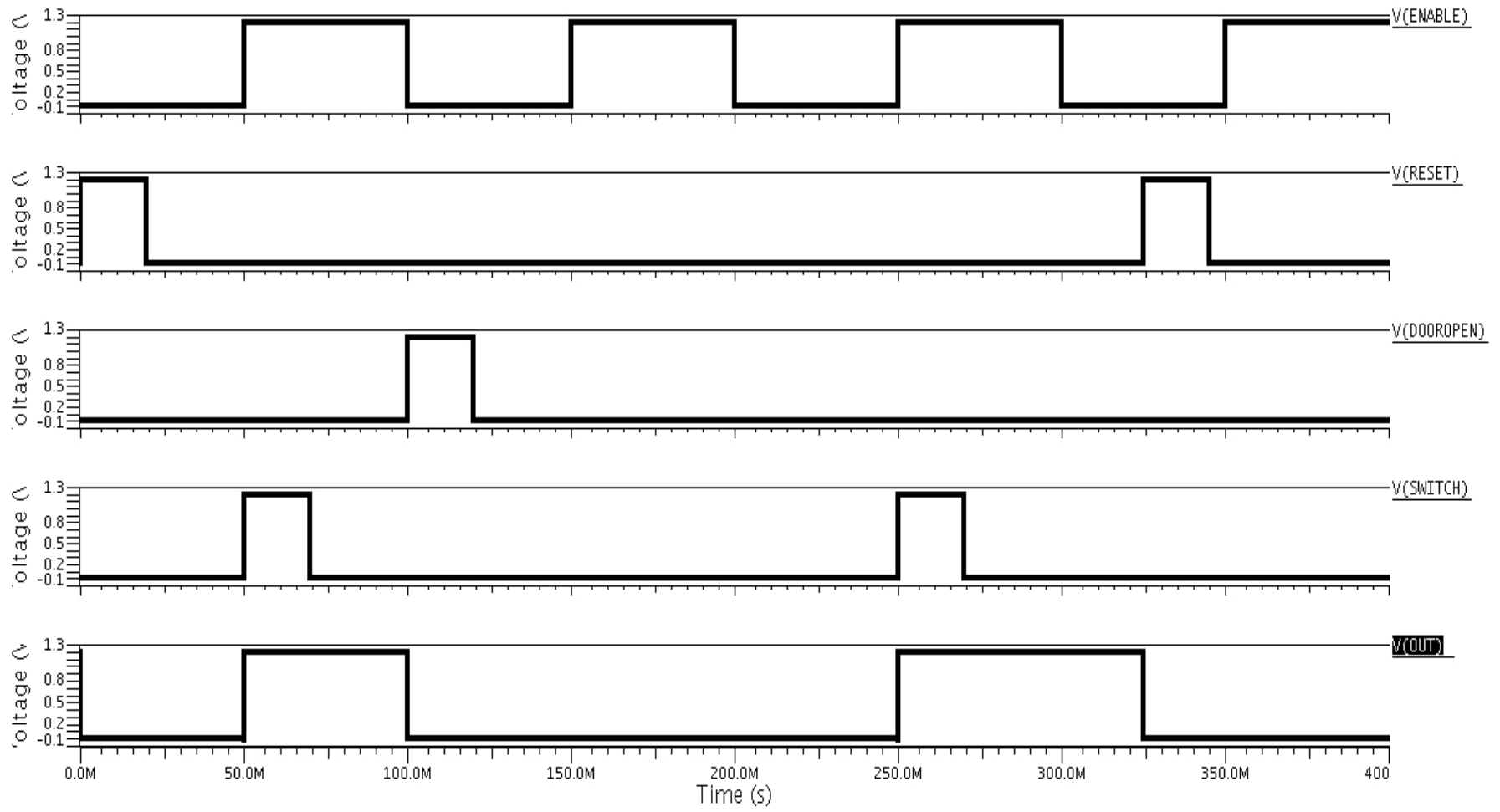


Switch Controlled Latch

- Enabled by clock timer.
- Read in data bits from keypad outputs.
- Latches are reset by the start button or the door open signal.



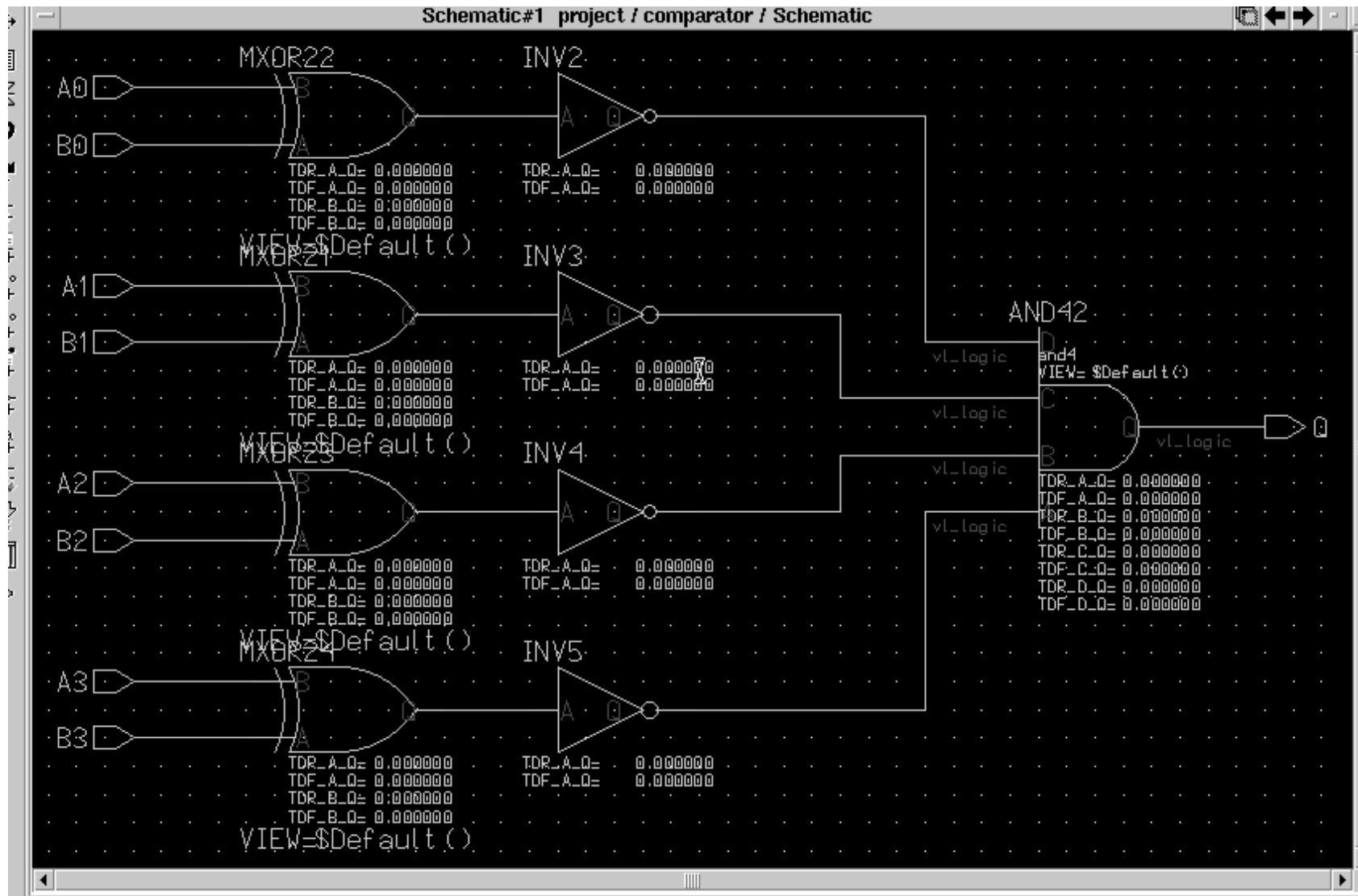
Switch Controlled Latch Sim



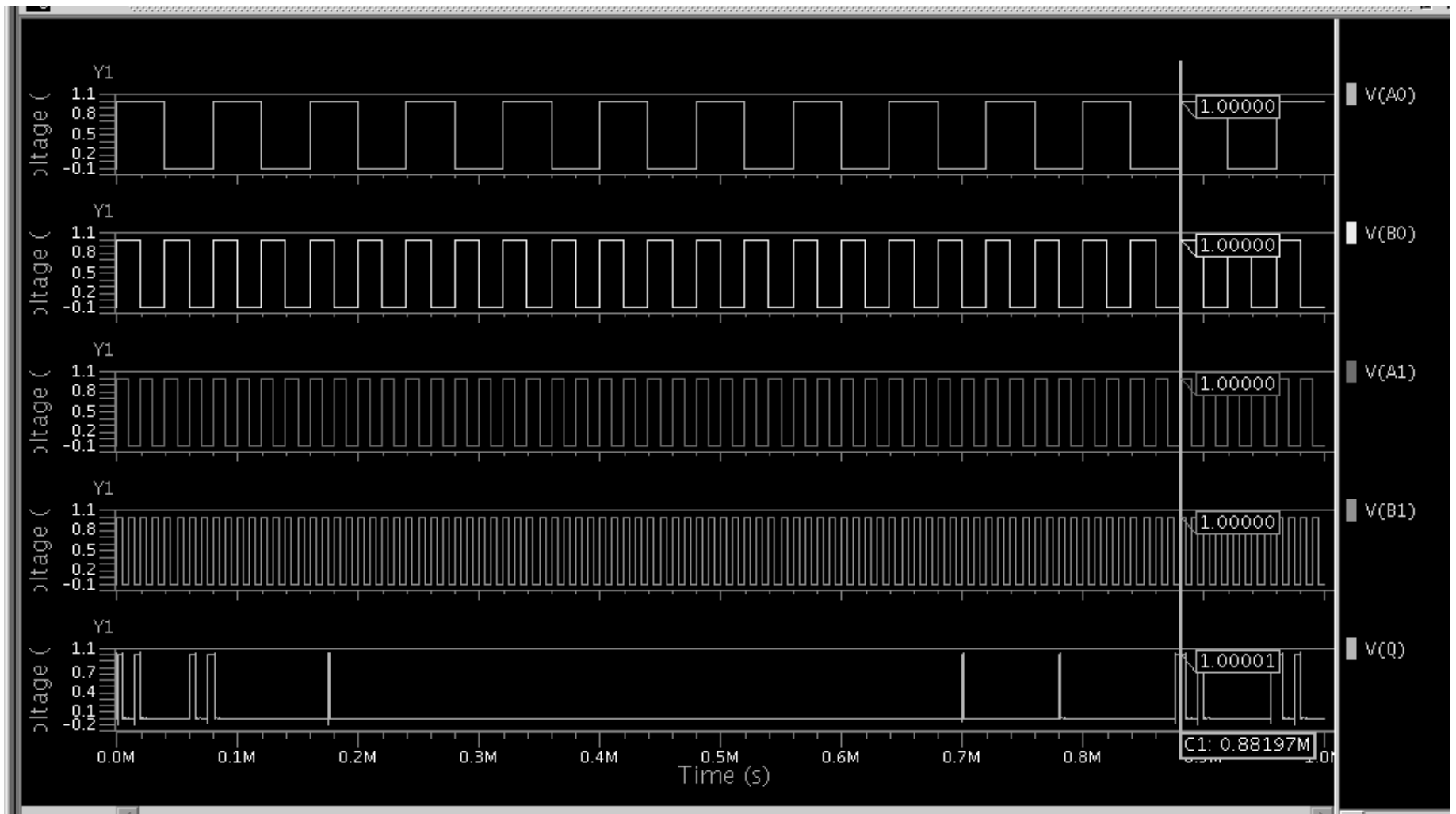
Comparator Circuit

- Compares data from Keypad latches with the pre-stored data to verify the entry code.
- Also used to customize enable set time.
- System utilizes four 4-bit Xnor comparator circuits and outputs the door commands.
- Each user register requires a separate comparator.

Comparator Circuit



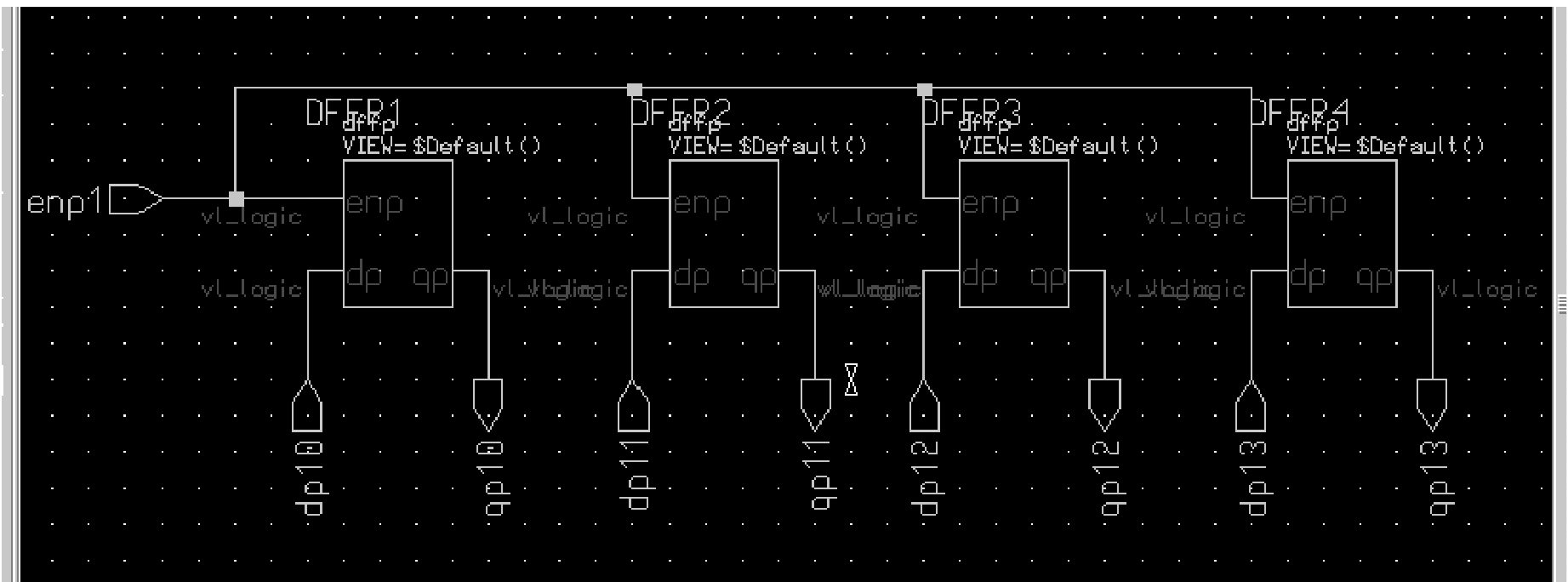
Comparator Simulation



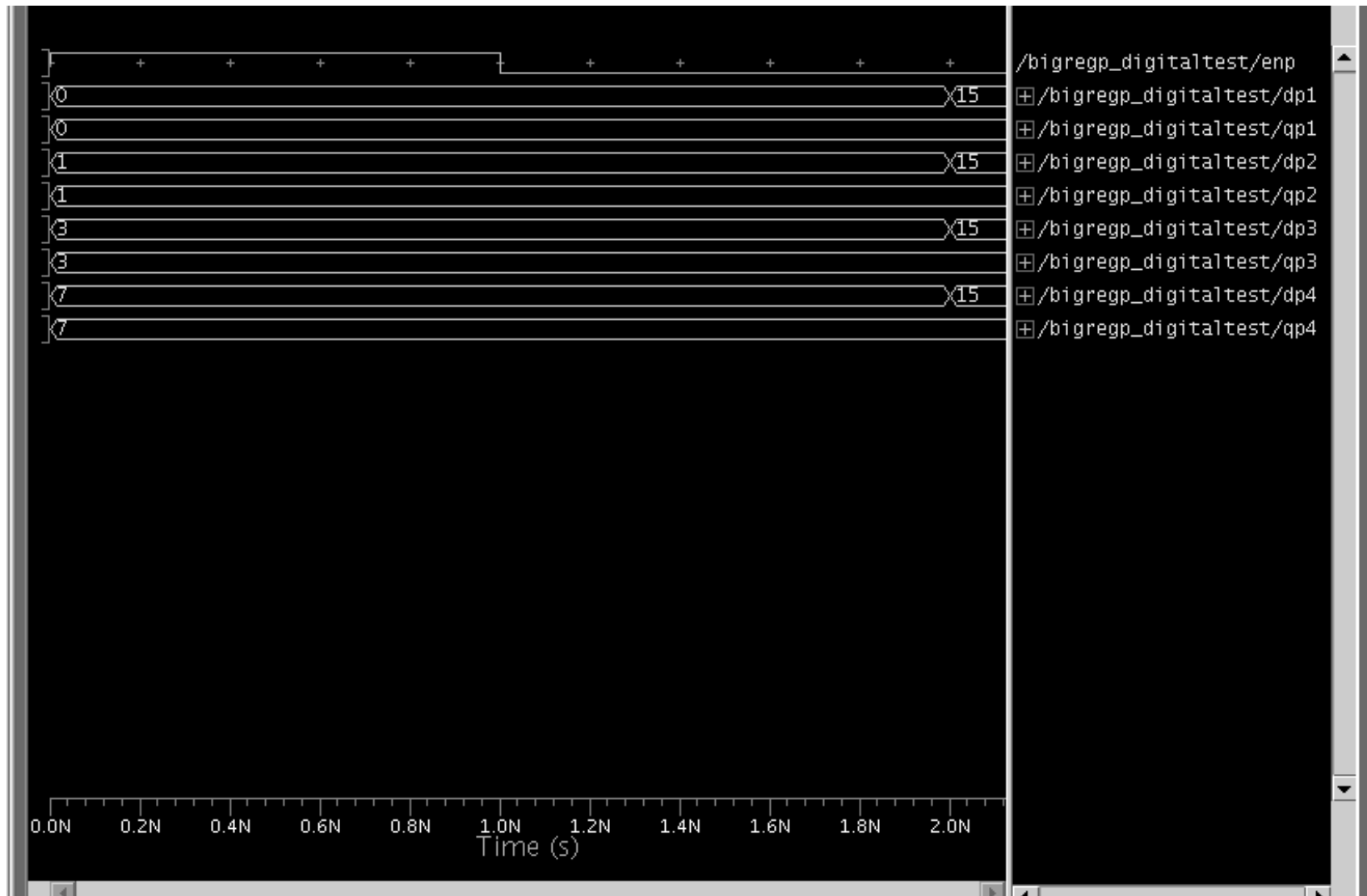
User Code Register

- Allows user to choose the register sets for programming user codes.
- Holds 4 bit binary code for comparison to keyed user codes.

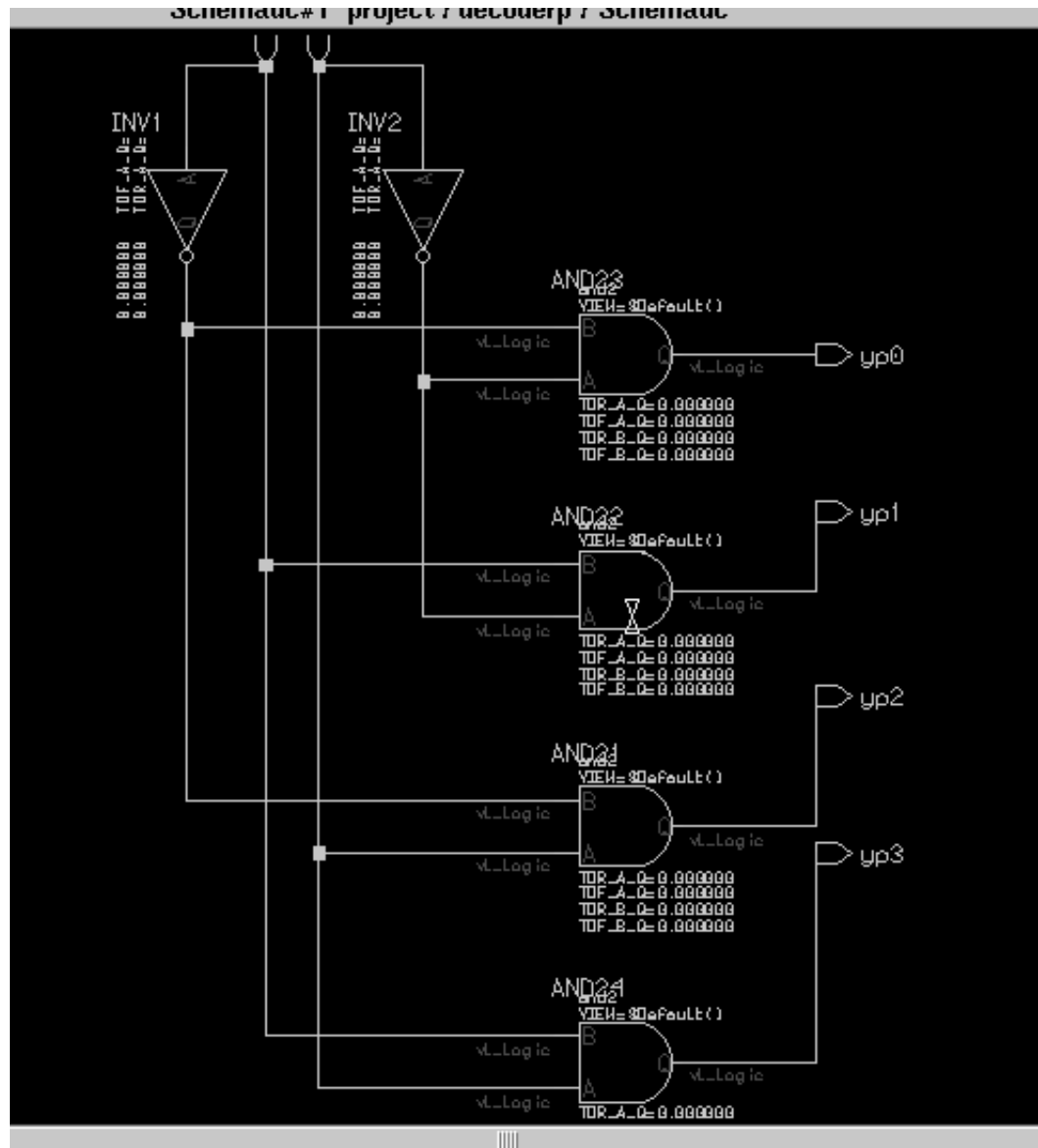
User Code Register Schematic



User Code Register Sim

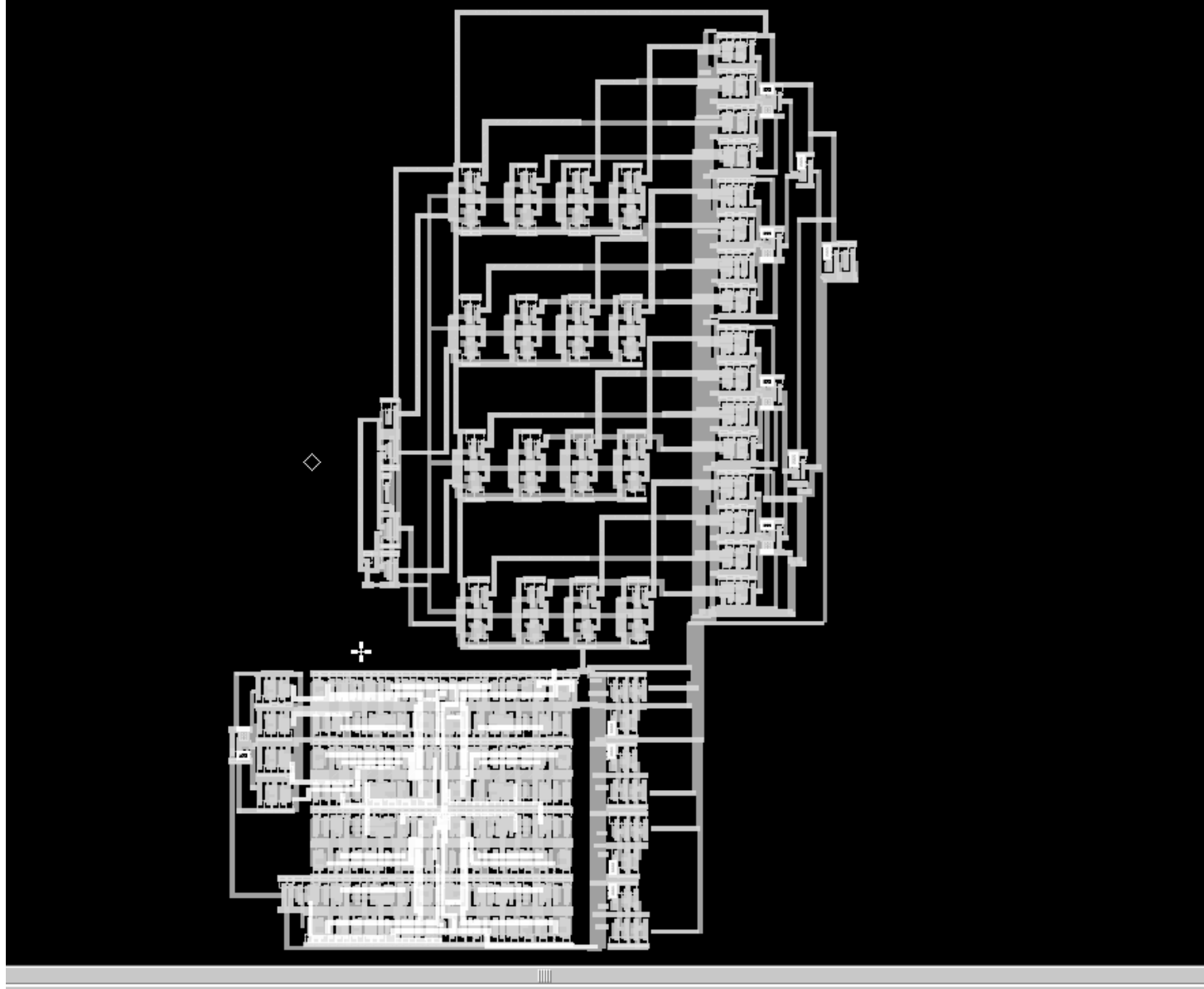


Decoder Schematic



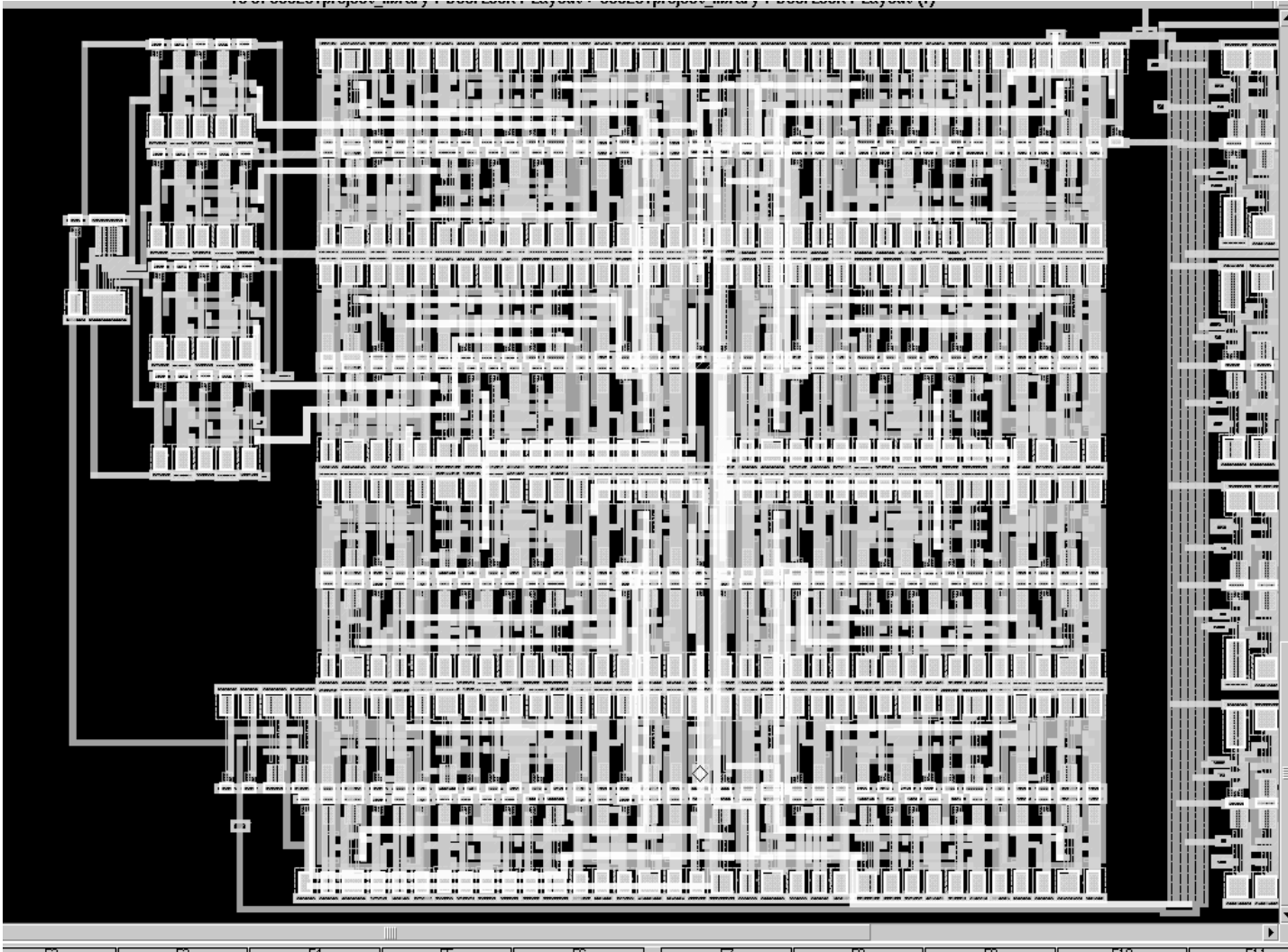
IC layout

IC 0: ece261project_library / DoorLock / Layout > ece261project_library / DoorLock / Layout (i)



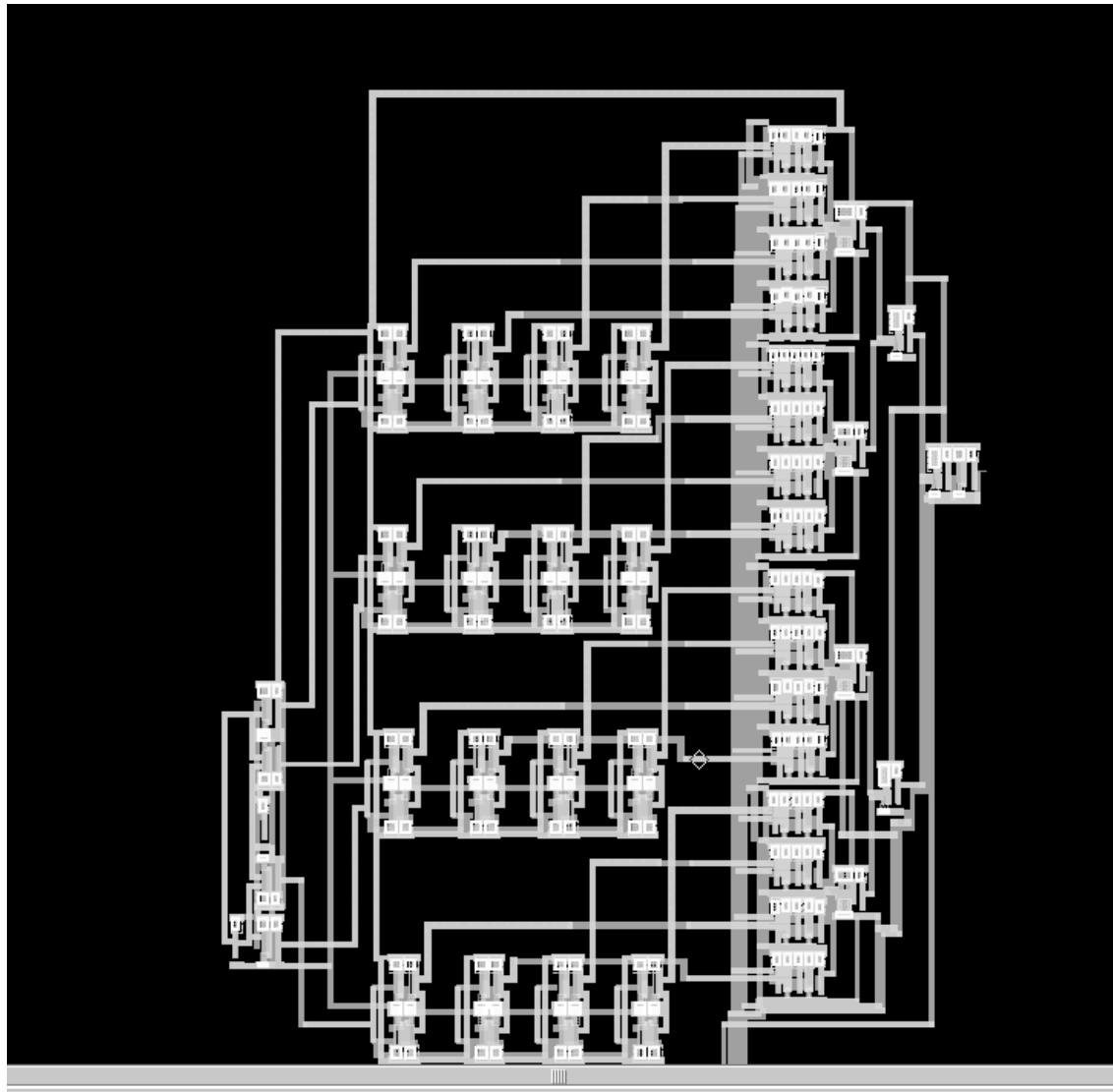
Top Cell

IC layout



Timer Cell
with key
latches

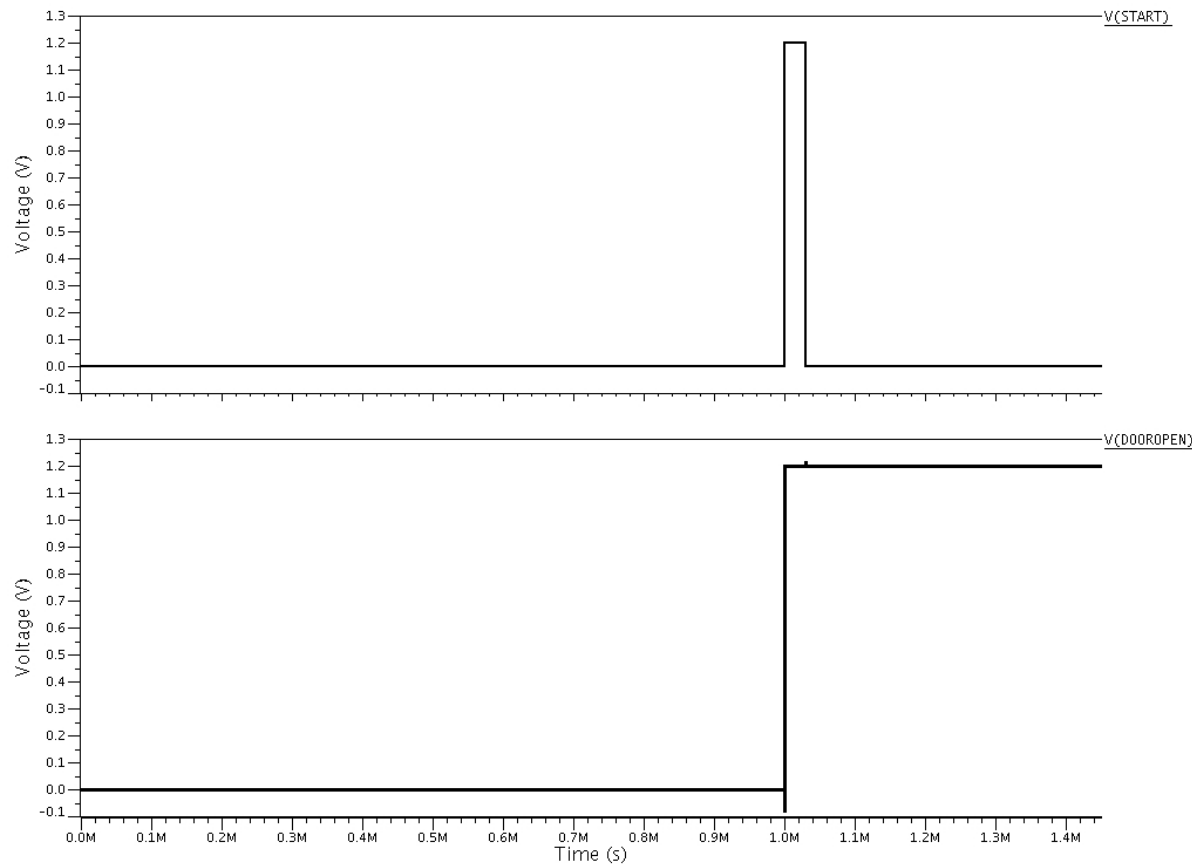
IC layout



Code storage
register and
comparator

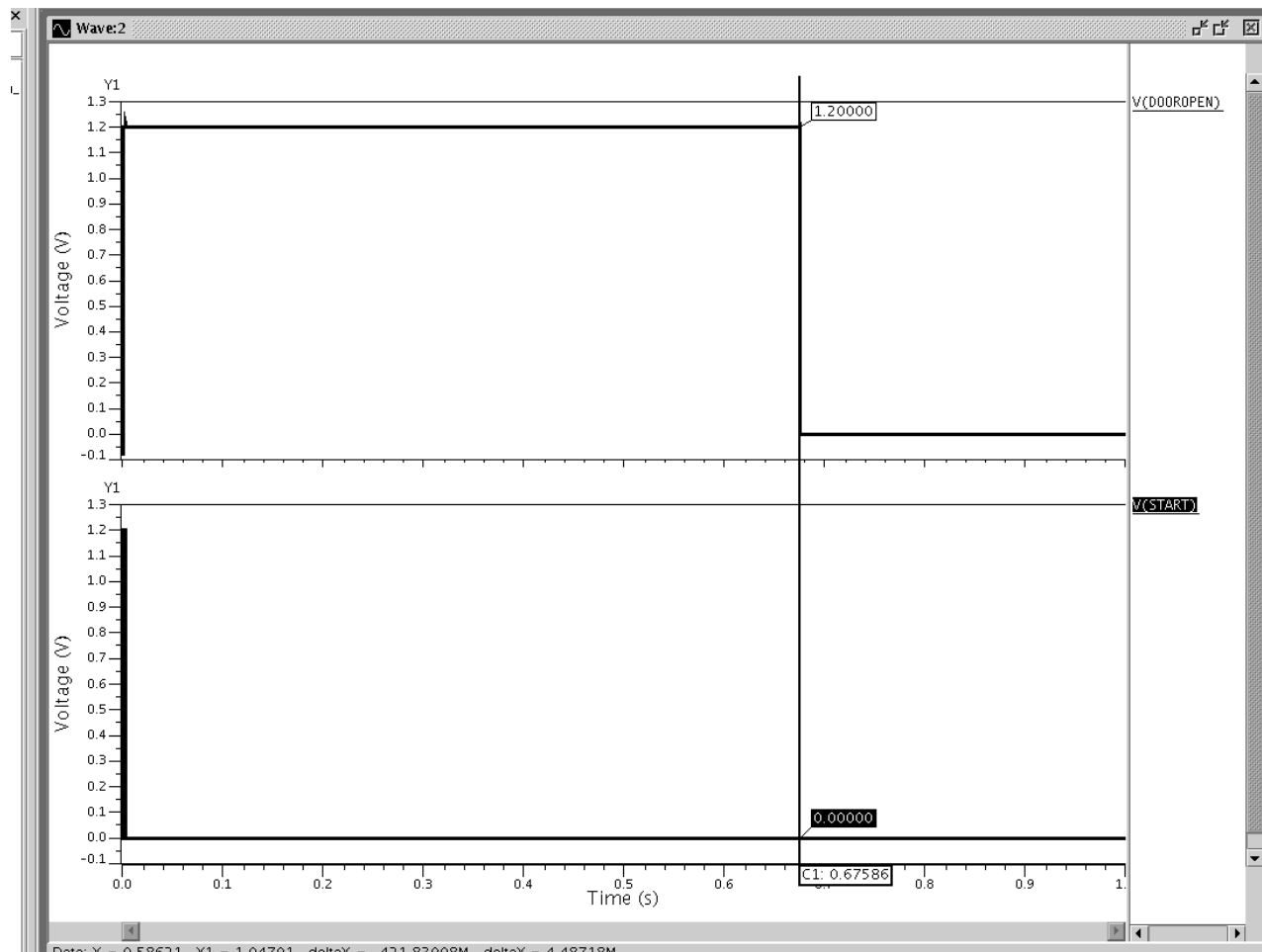
Top level analogue simulations

- Program one register and input matching key code (only start and door open signal shown for ease of view)



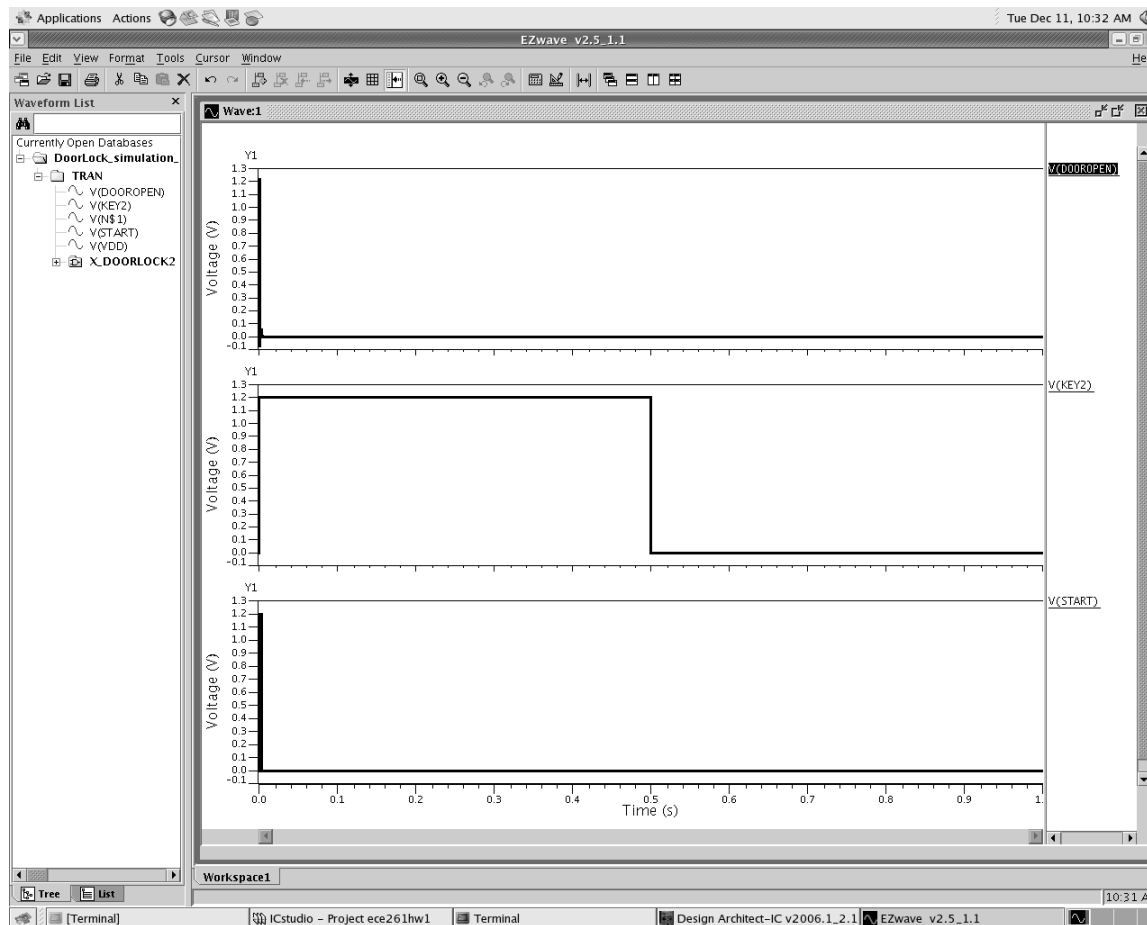
Top level analogue simulations

- Program one register and input matching key code door is unlocked for the chosen timer interval



Top level analogue simulations

- Program one register and input mismatch key code and attempt to change code mid cycle
- Door remains locked



Updated Power Consumption

- Proposed transistor count was 634.
- Current schematics include +1400 transistors.
- Simulated power usage was 135nW per enable cycle